ISO/IEC JTC1/SC17 2008-06-12
Cards and personal identification

ISO/IEC JTC1/SC17 N 3502 **WG8 N 1455**

DOCUMENT TYPE: Notification of Ballot

TITLE: Notification of Ballot: ISO/IEC CD 10373-6 (Revision) - Identification cards - Test methods - Part 6: Proximity cards

BACKWARD POINTER:

SOURCE: SECRETARIAT ISO/IEC JTC1/SC17

STATUS: This ballot has been posted to the ISO Electronic balloting application and is available under the Balloting Portal, Committee Internal Balloting.

ACTION ID: FYI

WORK ITEM: 1.17.2.6.

DUE DATE: 2008-09-11

DISTRIBUTION: P and L-Members of ISO/IEC JTC1/SC17
JTC1 Secretariat
ISO/IEC ITTF

MEDIUM: SERVER

NO. OF PAGES: 177

Secretariat ISO/IEC JTC1/SC17, APACS, Mercury House, Triton Court, 14 Finsbury Square, London EC2A 1LQ, England;
Telephone +44 (0)20 7711 6255; Fax: +44 (0)20 7711 6299; e-mail: chris.starr@apacs.org.uk

ISO/IEC JTC 1/SC 17 N 3xxx

Date: 2008-04-25

ISO/IEC CD 10373-6

ISO/IEC JTC 1/SC 17/WG 8

Secretariat: DIN

Identification cards — Test methods — Part 6: Proximity cards

Cartes d'identification — Méthodes d'essai — Partie 6: Cartes de proximité

Document type: International Standard
Document subtype:
Document stage: (30) Committee
Document language: E

J:\To_Do_WG8\wg8n1440_Draft_text_of_CD10373-6.doc STD Version 2.1c2

Contents

Foreword

ISO (the International Organization for Standardization) and IEC (the International Electrotechnical Commission) form the specialized system for worldwide standardization. National bodies that are members of ISO or IEC participate in the development of International Standards through technical committees established by the respective organization to deal with particular fields of technical activity. ISO and IEC technical committees collaborate in fields of mutual interest. Other international organizations, governmental and non-governmental, in liaison with ISO and IEC, also take part in the work. In the field of information technology, ISO and IEC have established a joint technical committee, ISO/IEC JTC 1.

International Standards are drafted in accordance with the rules given in the ISO/IEC Directives, Part 2.

The main task of the joint technical committee is to prepare International Standards. Draft International Standards adopted by the joint technical committee are circulated to national bodies for voting. Publication as an International Standard requires approval by at least 75 % of the national bodies casting a vote.

Attention is drawn to the possibility that some of the elements of this document may be the subject of patent rights. ISO and IEC shall not be held responsible for identifying any or all such patent rights.

ISO/IEC 10373-6 was prepared by Joint Technical Committee ISO/IEC JTC 1, *Information technology*, Subcommittee SC 17, Identification cards and related devices.

This second/third/... edition cancels and replaces the first/second/... edition (), [clause(s) / subclause(s) / table(s) / figure(s) / annex(es)] of which [has / have] been technically revised.

ISO/IEC 10373 consists of the following parts, under the general title *Identification cards — Test methods*:

— *Part 6: Proximity cards*

— *Part [n]:*

— *Part [n+1]:*

- — *Part 1: General characteristics tests*
- — *Part 2: Cards with magnetic stripes*
- — *Part 3: Integrated circuit(s) cards with contacts and related interface devices*
- — *Part 5: Optical memory cards*
- — *Part 6: Proximity cards*
- — *Part 7: Vicinity card*

The annexes B and F of this part of ISO/IEC 10373 are for information only.

Identification cards — Test methods — Part 6: Proximity cards

1 Scope

This International Standard defines test methods for characteristics of identification cards according to the definition given in ISO/IEC 7810. Each test method is cross-referenced to one or more base standards, which may be ISO/IEC 7810 or one or more of the supplementary standards that define the information storage technologies employed in identification cards applications.

NOTE 1 Criteria for acceptability do not form part of this International Standard but will be found in the International Standards mentioned above.

NOTE 2 Test methods described in this International Standard are intended to be performed separately. A given card is not required to pass through all the tests sequentially.

This part of ISO/IEC 10373 deals with test methods which are specific to contactless integrated circuit(s) card technology (Proximity cards). Part 1 of the standard, General characteristics, deals with test methods which are common to one or more ICC technologies and other parts deal with other technology-specific tests.

Unless otherwise specified, the tests in this part of ISO/IEC 10373 shall be applied exclusively to Proximity cards defined in ISO/IEC 14443-1, ISO/IEC 14443-2, ISO/IEC 14443-3 and ISO/IEC 14443-4.

2 Normative reference(s)

The following standards contain provisions which, through reference in this text, constitute provisions of this International Standard. At the time of publication, the editions indicated were valid. All standards are subject to revision, and parties to agreements based on this International Standard are encouraged to investigate the possibility of applying the most recent editions of the standards listed below. Members of ISO and IEC maintain registers of currently valid International Standards.

ISO/IEC 7810:1995, *Identification cards - Physical characteristics*

ISO/IEC 14443-1, *Identification cards - Proximity cards - Part 1: Physical characteristics*

ISO/IEC 14443-2, *Identification cards - Proximity cards - Part 2: Radio frequency power and signal interface*

ISO/IEC 14443-3, *Identification cards - Proximity cards - Part 3: Initialization and anticollision*

ISO/IEC 14443-4, *Identification cards — Contactless integrated circuit(s) cards — Proximity cards — Part 4: Transmission protocol*

IEC 61000-4-2: 1995, *Electromagnetic compatibility (EMC) - Part 4: Testing and measurement techniques - Clause 2: Electrostatic discharge immunity test*

ISBN 92-67-10188-9, 1993, *ISO Guide to the Expression of Uncertainty in Measurement*

3 Definitions, abbreviations and symbols

For the purposes of this document, the terms, definitions, abbreviations and symbols given in ISO/IEC 14443-2, ISO/IEC 14443-3, ISO/IEC 14443-4 and the following apply.

NOTE Elements in bold square brackets **[ ]** are optional Definitions.

3.1 Definitions

3.1.1
base standard

the standard which the test method is used to verify conformance to

3.1.2
Class 1 PICC

PICC whose antenna is located within a zone defined by two rectangles as seen in Figure 1 — PICC antenna zone:

— external rectangle: 81 mm × 49 mm.

— internal rectangle: 64 mm × 34 mm, centred in external rectangle, with 3 mm radius.

except from its connection endings with a maximum area of 300 mm^2.

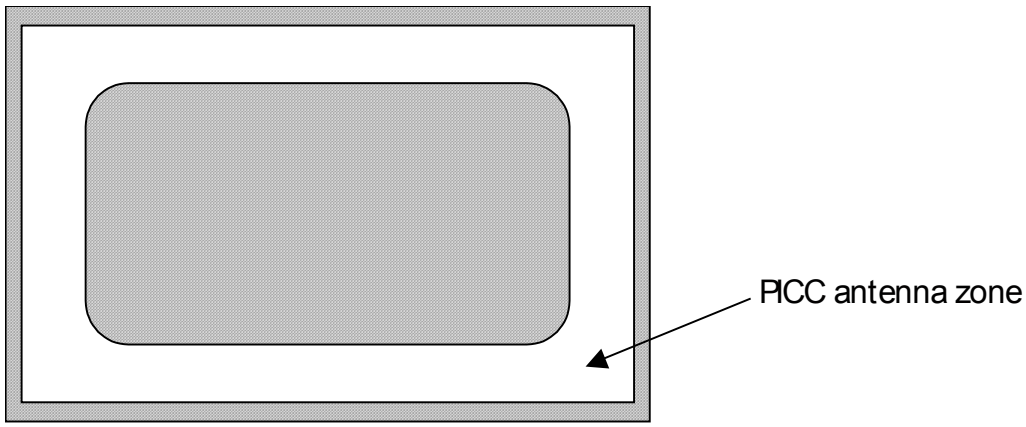


Figure 1 — PICC antenna zone

WARNING — The "Class 1" PICC shall also pass the "Class 1" PICC maximum loading effect test defined in 7.4.

3.1.3
test method

a method for testing characteristics of identification cards for the purpose of confirming their compliance with International Standards

3.1.4
CascadeLevels

number of cascade levels of the PICC

3.1.5
Command Set

set describing the PICC commands during initialization and anticollision

NOTE See ISO/IEC 14443-3:2001, 6.3 for PICC Type A and ISO/IEC 14443-3:2001, 7.5 for PICC Type B.

3.1.6
Mute

no response within a specified timeout, e.g. expiration of FWT

3.1.7
PICC States

different PICC states during initialization and anticollision

NOTE See ISO/IEC 14443-3:2001, 6.2 for PICC Type A and ISO/IEC 14443-3:2001, 7.4 for PICC Type B.

3.1.8
Scenario

defined typical protocol and application specific communication to be used with the test methods defined in this part of ISO/IEC 10373

3.1.9
State Transition Map

map describing all possible state transitions, i.e. the map:

PICC States $\times$ Command Set $\rightarrow$ PICC States

3.1.10
Test Initial State (TIS)

element from PICC States that is the PICC state before performing a specific PICC command from Command Set

3.1.11
Test Target State (TTS)

element from PICC States that is the PICC state after performing a specific PICC command from Command Set

3.2 Abbreviations and symbols

$I(c)_n$**(**inf **[**,CID=cid**] [**,NAD=nad**]** **[**,~CRC**])**	ISO/IEC 14443-4 I-block with chaining bit c∈{1,0}, block number n∈{1,0} and information field inf. By default no CID and no NAD will be transmitted. If CID=cid∈{0...15} is specified, it will be transmitted as second parameter. If NAD=nad∈{0...'FF'} is specified it will be transmitted as third parameter. If the literal '~CRC' is not specified, a valid CRC corresponding to the type of the PICC will be transmitted by default (i.e. CRC_A or CRC_B)

(xxxxx)b	Data bit representations
'XY'	Hexadecimal notation, equal to XY in base 16
ATA(cid)	Answer to ATTRIB, i.e. (mbli+cid CRC_B), with mbli an arbitrary hex value (see ISO/IEC 14443-3:2001, 7.11)
ATTRIB(cid, fsdi)	Default ATTRIB command with PUPI from ATQB, CID=cid and Maximum Frame Size Code value = fsdi i.e. ('1D' PUPI cid fsdi '01 00' CRC_B)
BCC	The one byte block checksum as described in ISO/IEC 14443-3 by Block Check Character(UID CLn check byte), Type A
CRC	Cyclic Redundancy Check
CRC_A	Cyclic Redundancy Check, as defined for the PICC Type A in ISO/IEC 14443-3
CRC_B	Cyclic Redundancy Check, as defined for the PICC Type B in ISO/IEC 14443-3
DUT	Device under test
ESD	Electrostatic Discharge
FWT	Frame waiting time
FWT_{TEMP}	Temporary frame waiting time
Fc	Frequency of the operating field
fcm	Frequency of the operating field during the PICC load modulation test
Fs	Frequency of the subcarrier
H	Field strength of the PCD antenna field
H_{max}	Maximum fieldstrength of the PCD antenna field
H_{min}	Minimum fieldstrength of the PCD antenna field
IUT	Implementation Under Test (ISO/IEC 9646), within the scope of this document IUT represents the PCD under the test
LT	Lower Tester (ISO/IEC 9646), the PICC-emulation part of the PCD-test-apparatus
m	Modulation index as defined in 3.3 of ISO/IEC 14443-2:2001, 3.3
Mute	No response within a specified timeout
PCD	Proximity Coupling Device
PICC	Proximity Card
PPS(cid, dri, dsi)	Default PPS request with CID=cid, DRI=dri and DSI=dsi, i.e. (‘D'+cid '11‘ dsi x 4 + dri CRC_A)
R(ACK **[**,CID=cid**] [**,~CRC**]**)$_n$	ISO/IEC 14443-4 R(ACK) Block with block number n. The definition of the optional CID and ~CRC symbols is as described in the I(c)$_n$ block above

R(NAK **[**,CID=cid**][**,~CRC**])**$_n$	ISO/IEC 14443-4 R(NAK) Block with block number n. The definition of the optional CID and ~CRC symbols is as described in the I(c)$_n$ block above
RATS(cid, fsdi)	Default RATS command with CID=cid and FSDI value = fsdi i.e. (' E0' fsdi x 16+cid CRC_A)
READY(l)	READY state in cascade level l, l ∈ {1, 2, 3}; i. e. READY(2) is a PICC cascade level 2
READY*(l)	READY* state in cascade level l, l ∈ {1, 2, 3}; i. e. READY*(2) is a PICC cascade level 2
REQB(N)	REQB command with N as defined in ISO/IEC 14443-3:2001, 7.7.4
S(WTX)(n [,CID=cid][,~CRC])	ISO/IEC 14443-4 S(WTX) block with parameter WTXM= n. The definition of the optional CID and ~CRC symbols is as described in the I(c)$_n$ block above
S(DESELECT **[**,CID=cid**]** **[**,~CRC**]**)	ISO/IEC 14443-4 S(DESELECT) block. The definition of the optional CID and ~CRC symbols is as described in the I(c)$_n$ block above
SAK(cascade)	the SELECT(l) answer with the cascade bit (bit 3) set to 1
SAK(complete)	the SELECT(l) answer with the cascade bit (bit 3) set to 0
SEL(c)	Select code of level c (i.e. SEL(1) = '93', SEL(2) = '95', SEL(3) = '97')
SELECT(l)	SELECT command of cascade level l, i.e. SELECT(1) = ('93 70' UIDTX$_1$ BCC CRC_A) SELECT(2) = ('95 70' UIDTX$_2$ BCC CRC_A) SELECT(3) = ('97 70' UIDTX$_3$ BCC CRC_A) Select cascade level l command where l is equal to 1, 2 or 3
SFGI	Start-up Frame Guard Time
SLOTMARKER(n)	Slot-MARKER command with slot number n, i.e. (16 x (n-1)+5 CRC_B)
t1, t2, t3	Pause A length, Pause A “Low” time and Pause A rise time, as defined, respectively, in ISO/IEC 14443-2
TB-PDU	Transmission Block Protocol Data Unit, which consists of either I-block, R-block or S-block
TEST_COMMAND1(1)	Default test command consisting of one unchained I-block Note: This command depends on the negotiated maximum frame size value of the PICC
TEST_COMMAND1(n)$_k$	INF field of k'th I-block chain of TEST_COMMAND1(n) Note: This I-block depends on the negotiated maximum frame size value of the PICC
TEST_COMMAND1(n), n > 1	Default test command consisting of n chained I-blocks. (PCD chaining) Note: This command depends on the negotiated maximum frame size value of the PICC
TEST_COMMAND2(n), n > 1	Default test command which expects a response consisting of n chained I-blocks Note: This command depends on the negotiated maximum frame size value of the PCD.

TEST_COMMAND3	Default test command consisting of one I-block which needs between n x FWT and (n+1) x FWT time for execution
TEST_RESPONSE1(n)	INF field of the response to TEST_COMMAND1(n). This response is assumed to be always unchained
TEST_RESPONSE2(n)	Response to TEST_COMMAND2(n) Note: This I-block depends on the negotiated maximum frame size value of the PCD.
$TEST\_RESPONSE2(n)_k$	INF field of k'th I-block chain of TEST_RESPONSE2(n) Note: This I-block depends on the negotiated maximum frame size value of the PCD.
TEST_RESPONSE3	Response I-block to TEST_COMMAND3. This response is always assumed to be unchained
Test Scenario	A defined typical protocol and application-specific communication to be used with the test methods defined in this document
TM- PDU	Test Management Protocol Data Unit (ISO/IEC 9646-1, PDU)
t_r, t_f	Carrier rise and fall times as defined, respectively, in Figure 12 of ISO/IEC 14443-2
UID	Unique Identifier, Type A
Uidn	Byte number *n* of Unique Identifier, $n \geq 0$
$UIDTX_n$	transmitted UID 32-bit data at cascade level n(see Table 1 — Mapping from UID to UIDTX)
UT	Upper Tester (ISO/IEC 9646), the master part of the PCD-test-apparatus
UT-APDU	Upper Tester Application Protocol Data Unit: a packet of data to be sent by the PCD to the LT through the RF interface
V_{LMA}	Load Modulation Amplitude
WUPB(N)	WUPB command with N as defined in ISO/IEC 14443-3:2001, 7.7.4
~X	Bit sequence consisting of the inverted bits of bit sequence X or any other bit sequence different from X
X[[a..b]]	Bit subsequence of bit sequence X consisting of the bits between position a and b included. If a > b then the sequence is empty
X[[n]]	Bit at position n of bit sequence X. First bit is at position 1
X[n]	Byte at position n of bit sequence X. First byte is at position 1 (i.e. X[n] = X[[(n-1) x 8+1..n x 8]])

Table 1 — Mapping from UID to UIDTX

Cascade level	Single UID PICC	Double UID PICC	Triple UID PICC
$UIDTX_1$	UID0 UID1 UID2 UID3	'88' UID0 UID1 UID2	'88' UID0 UID1 UID2
$UIDTX_2$	---	UID3 UID4 UID5 UID6	'88' UID3 UID4 UID5
$UIDTX_3$	---	---	UID6 UID7 UID8 UID9

4 Default items applicable to the test methods

4.1 Test environment

Unless otherwise specified, testing shall take place in an environment of temperature 23 °C ± 3 °C (73 °F ± 5 °F) and of relative humidity 40 % to 60 %.

4.2 Pre-conditioning

Where pre-conditioning is required by the test method, the identification cards to be tested shall be conditioned to the test environment for a period of 24 h before testing.

4.3 Default tolerance

Unless otherwise specified, a default tolerance of ± 5 % shall be applied to the quantity values given to specify the characteristics of the test equipment (e.g. linear dimensions) and the test method procedures (e.g. test equipment adjustments).

4.4 Spurious Inductance

Resistors and capacitors should have negligible inductance.

4.5 Total measurement uncertainty

The total measurement uncertainty for each quantity determined by these test methods shall be stated in the test report.

Basic information is given in ”ISO Guide to the Expression of Uncertainty in Measurement”, ISBN 92-67-10188-9, 1993.

5 Apparatus and circuits for test of ISO/IEC 14443-1 and ISO/IEC 14443-2 parameters

This clause defines the test apparatus and test circuits for verifying the operation of a PICC or a PCD according to ISO/IEC 14443-1 and ISO/IEC 14443-2. The test apparatus includes:

- Measurement instruments (see 5.1)
- Calibration coil (see 5.2)
- Test PCD assembly (see 5.3)
- Reference PICC (see 5.4)

These are described in the following clauses.

5.1 Minimum requirements for measurement instruments

5.1.1 Oscilloscope

The digital sampling oscilloscope shall be capable of sampling at a rate of at least 500 million samples per second with a resolution of at least 8 bits at optimum scaling and shall have a minimum bandwidth of 500 MHz. The oscilloscope should have the capability to output the sampled data as a text file to facilitate mathematical and other operations such as windowing on the sampled data using external software programmes (see Annex F).

5.2 Calibration coil

This clause defines the size, thickness and characteristics of the calibration coil.

5.2.1 Size of the Calibration coil card

The calibration coil card shall consist of an area which has the height and width of an ID-1 type defined in ISO/IEC 7810 containing a single turn coil concentric with the card outline (see Figure 2 — Calibration coil).

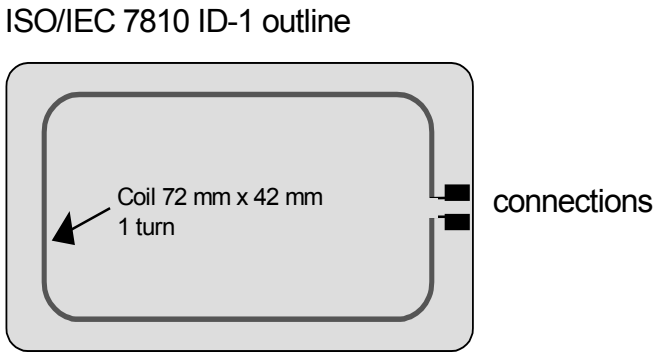


Figure 2 — Calibration coil

5.2.2 Thickness and material of the Calibration coil card

The thickness of the calibration coil card shall be 0,76 mm ±10%. It shall be constructed of a suitable insulating material.

5.2.3 Coil characteristics

The coil on the calibration coil card shall have one turn. The outer size of the coil shall be 72 mm x 42 mm with corner radius 5 mm. Relative dimensional tolerance shall be ± 2 %.

NOTE The area over which the field is integrated is approximately 3000 mm^2.

The coil shall be made as a printed coil on printed circuit board (PCB) plated with 35 µm copper. Track width shall be 500 µm with a relative tolerance of ± 20 %. The size of the connection pads shall be 1,5 mm x 1,5 mm.

NOTE At 13,56 MHz the approximate inductance is 250 nH and the approximate resistance is 0,4 Ω.

A high impedance oscilloscope probe (e.g. >1MΩ, <14pF) shall be used to measure the (open circuit) voltage induced in the coil. The resonance frequency of the calibration coil and connecting leads shall be above 60 MHz.

NOTE A parasitic capacitance of the probe assembly of less than 35 pF normally ensures a resonant frequency for the whole set of greater than 60 MHz.

The open circuit calibration factor for this coil is 0,32 Volts (rms) per A/m (rms). [Equivalent to 900 mV (peak-to-peak) per A/m (rms)]

NOTE The high impedance oscilloscope probe ground connection should be as short as possible, less than 20 mm or coaxial connection.

5.3 Test PCD assembly

The test PCD assembly shall consist of a 150 mm diameter PCD antenna and two parallel sense coils: sense coil a and sense coil b. The test set-up is shown in Figure 3 — Test set-up (principle). The sense coils shall be connected such that the signal from one coil is in opposite phase to the other. The 10 Ω potentiometer P1 serves to fine adjust the balance point when the sense coils are not loaded by a PICC or any magnetically coupled circuit. The capacitive load of the probe including its parasitic capacitance shall be less than 14 pF.

NOTE 1 The capacitance of the connections and of the oscilloscope probe should be kept to a minimum for reproducibility.

NOTE 2 In order to avoid any unintended misalignment in case of an unsymmetrical set-up the tuning range of the potentiometer P1 is only 10 Ω. If the set-up cannot be compensated by the 10 Ω potentiometer P1 the overall symmetry of the set-up should be checked.

NOTE 3 The high impedance oscilloscope probe ground connection should be as short as possible, less than 20 mm or coaxial connection.

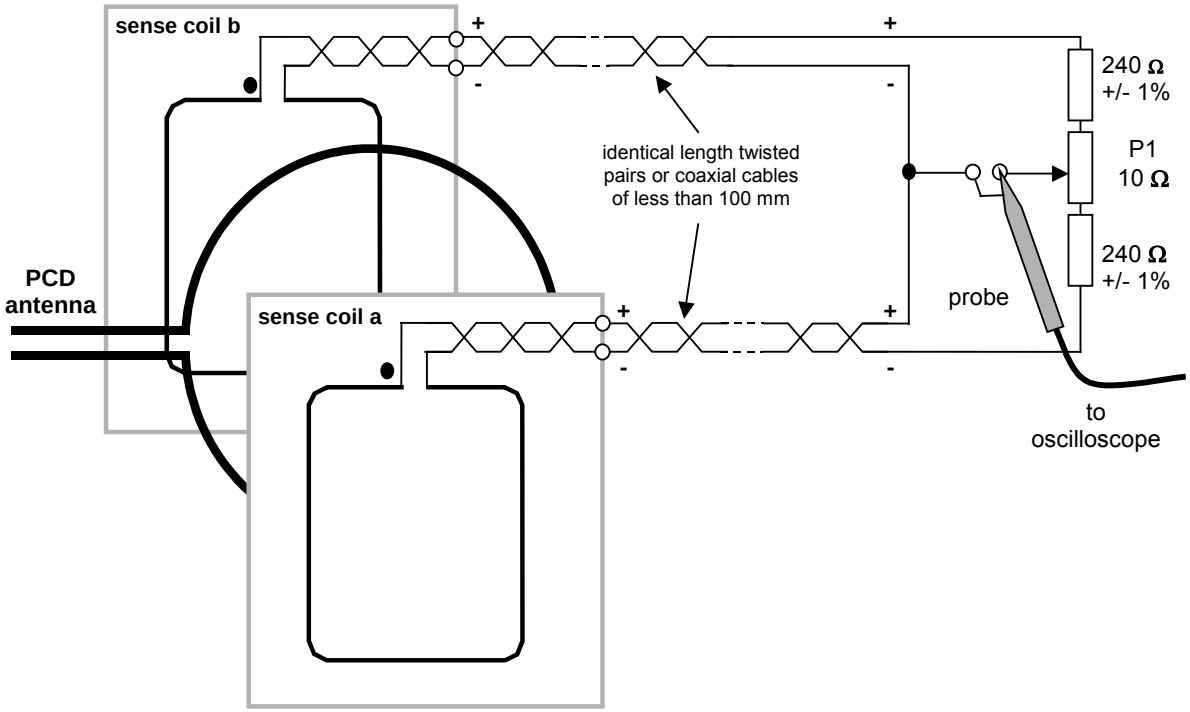


Figure 3 — Test set-up (principle)

5.3.1 Test PCD antenna

The Test PCD antenna shall have a diameter of 150 mm and its construction shall conform to the drawings in Annex A.

The matching of the PCD antenna should be accomplished by using an impedance analyzer or a network analyzer. If either an impedance analyzer or a network analyzer is not available, then the matching may be accomplished with the procedure given in Annex B.

5.3.2 Sense coils

The size of the sense coils shall be 100 mm x 70 mm. The sense coil construction shall conform to the drawings in Annex C.

5.3.3 Assembly of Test PCD

The sense coils and Test PCD antenna shall be assembled parallel and with the sense and antenna coils coaxial and such that the distance between the active conductors is 37,5 mm as in Figure 4 — Test PCD assembly. The dimensional tolerance shall be better than ± 0,5 mm. The distance between the coil in the DUT and the calibration coil shall be equal with respect to the coil of the test PCD antenna.

NOTE These distances are chosen to represent the typical operating distance of the PICC.

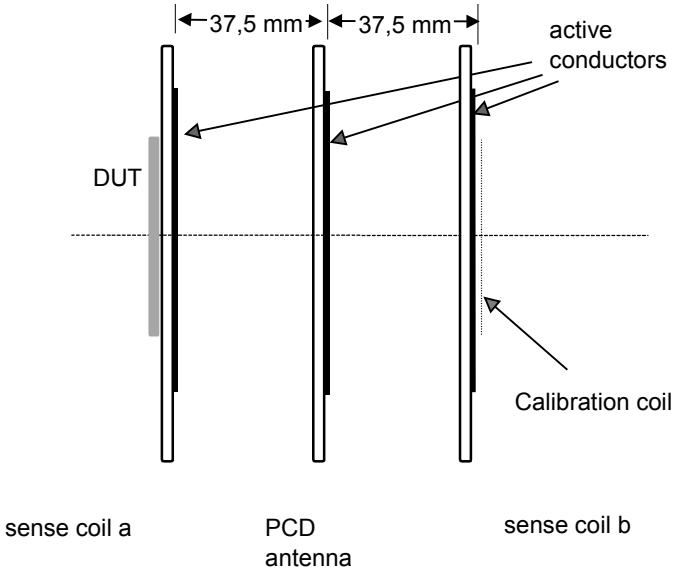


Figure 4 — Test PCD assembly

5.4 Reference PICC

A Reference PICC is defined to test the ability of a PCD to:

— generate a field strength of at least H_{min} and not exceeding H_{max}
— transfer power to a PICC
— transmit a modulated signal to a PICC
— receive a load modulation signal from the PICC

in its operating volume.

5.4.1 Dimensions of the Reference PICC

The Reference PICC shall consist of an area containing the coils which has the height and width defined in ISO/IEC 7810 for ID-1 type. An area external to this, containing the circuitry which emulates the required PICC functions, shall be appended in such a way as to allow insertion into the test set-ups and so as to cause no interference to the tests. The dimensions shall be as in **Fehler! Verweisquelle konnte nicht gefunden werden.**.

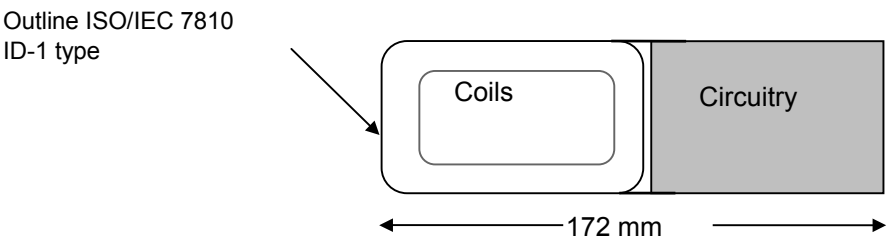


Figure 5 — Reference PICC dimensions

5.4.2 Thickness of the Reference PICC board

The thickness of the Reference PICCs active area shall be 0,76 mm ±10%.

5.4.3 Coil characteristics

The main coil in the active area of the Reference PICC shall have 4 turns and shall be concentric with the area outline.
The outer size of the main coil shall be 72 mm x 42 mm with a relative tolerance of ± 2 %.
The main coil shall be printed on a printed circuit board (PCB) plated with 35 µm copper.
Track width and spacing shall be 500 µm with a relative tolerance of ± 20 %.

The pick-up coil in the active area shall have track width of 500 µm and a layout as defined in Annex D.

5.4.4 Circuit diagram

The Reference PICC shall have a circuit diagram as defined in Figure 6 — Reference PICC circuit diagram.

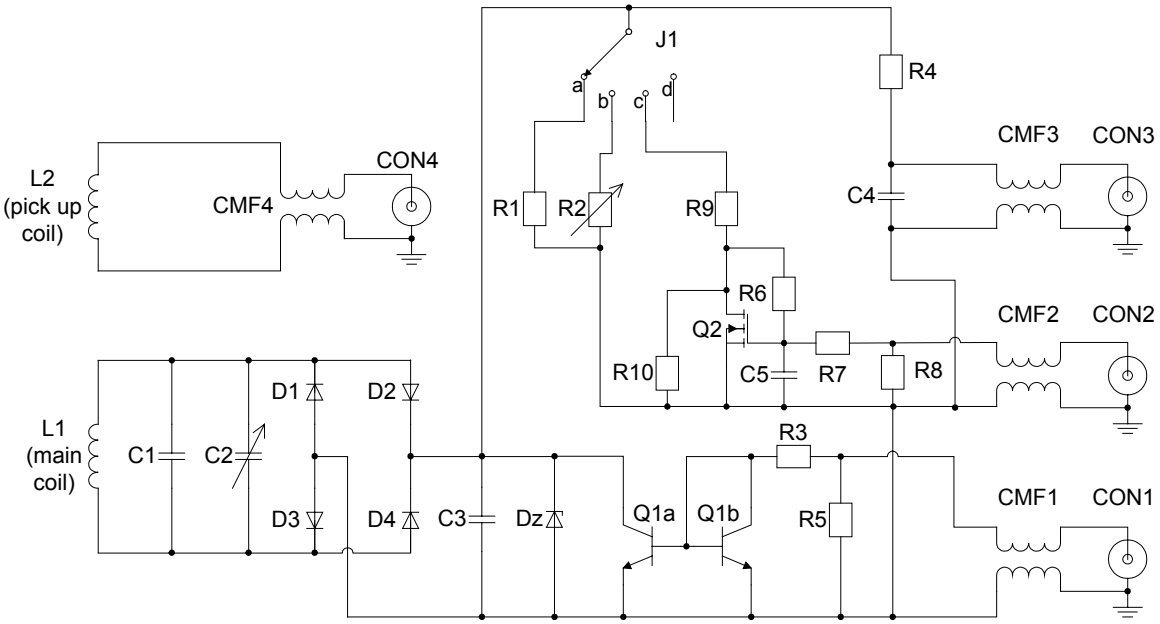


Figure 6 — Reference PICC circuit diagram

Table 2 — Reference PICC components list

Component	Value	Component	Value
L1	See Annex D	C1	10 pF
L2	See Annex D	C2	5 pF – 30 pF
R1	1.8 kΩ	C3	27 pF
R2	0 kΩ – 5 kΩ	C4	1 nF
R3	1 kΩ	C5	1 nF
R4	51 kΩ	D1, D2, D3, D4	BAR43 or equivalent [a]
R5	51 Ω	Dz	BZX84, 10V or equivalent [a]
R6	270 kΩ	Q1	BCV61V or equivalent
R7	110 kΩ	Q2	BSS83 or equivalent

Component	Value	Component	Value
R8	51 Ω	CMF1, CMF2, CMF3, CMF4	ACM3225 -102-2P or equivalent
R9	130 Ω	CON1, CON2, CON3, CON4	
R10	5,1 kΩ		
[a] Care should be taken on parameters Cj (Junction capacitance), Cp (Package capacitance), Ls (Series inductance) and Rs (series resistance) of equivalent diodes. Note that these values may not be available in the datasheet.			

NOTE 1 Position 'd' of jumper J1 is RFU.

NOTE 2 At 13,56 MHz the inductance of L1 is 2,3 µH ± 10 % and the resistance is 1,8 **Ω**. ± 5 %.

NOTE 3 At 13,56 MHz the inductance of L2 is YYY nH ± 10 % and the approximate resistance is ZZZ **Ω** ± 5 %.

At CON1 the load modulation signal shall be applied. The load modulation can be determined in test PCD assembly. When not used, the load modulation signal generator shall be disconnected or set to 0V.

With the voltage at CON2 the RefPICC load can be adjusted until the required d.c. voltage shows at CON3.

The RefPICC d.c. voltage shall be measured at CON3 using a high impedance voltmeter and the connection wires should be twisted or coaxial.

The PCD waveform parameters are picked up at CON4 using a high impedance oscilloscope probe. The high impedance oscilloscope probe ground connection should be as short as possible, less than 20 mm or coaxial connection.

5.4.5 Reference PICC resonance frequency tuning

The Reference PICC resonance frequency shall be calibrated with the following procedure.

1) set jumper J1 to position a;

2) Connect the calibration coil directly to a signal generator and the Reference PICC connector CON3 to a high impedance voltmeter. Disconnect CON2 or set the applied voltage to 0 V;

3) Locate the Reference PICC at a distance d = 5 mm above the calibration coil with the axes of the two coils (calibration coil and Reference PICC main coil) being congruent (see Figure 7 — Reference PICC frequency tuning set-up (principle));

4) Drive the calibration coil with a sine wave set to the desired resonance frequency;

5) Adjust the Reference PICC capacitor C2 to get maximum d.c. voltage at CON3;

6) Adjust the signal generator drive level to read a d.c. voltage of 6 V at CON3;

7) Repeat steps 5 and 6 until the maximum voltage after step 5 is 6 V.

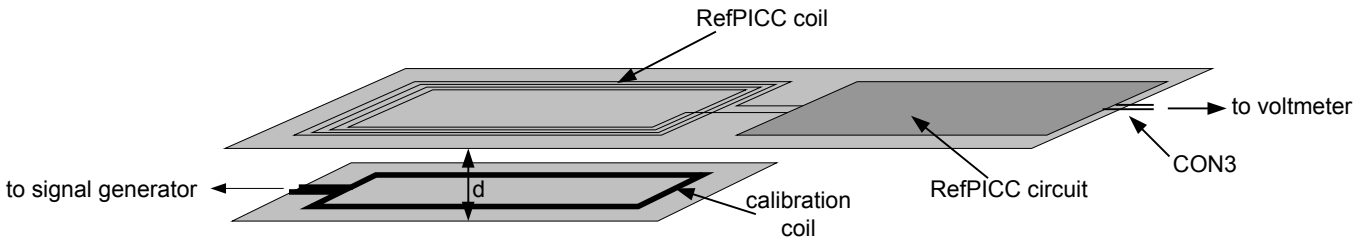


Figure 7 — Reference PICC frequency tuning set-up (principle)

6 Test of ISO/IEC 14443-1 parameters

6.1 PCD tests

6.1.1 Alternating magnetic field

6.1.1.1 Purpose

This test determines that the PCD generates a field not higher than the average value specified in ISO/IEC 14443-1, in any possible PICC position.

6.1.1.2 Test procedure

a) Tune the Reference PICC to 19 MHz as described in 5.4.5

b) Calibrate the Test PCD assembly to produce the average field value specified in ISO/IEC 14443-1 on the calibration coil.

c) Place the Reference PICC into the DUT position on the Test PCD assembly. Switch the jumper J1 to position 'b' and adjust R2 to obtain a d.c. voltage of 3 V measured at connector CON3. Alternatively, jumper J1 may be set to position 'c' and the applied voltage on CON2 is adjusted to obtain a d.c. voltage of 3 V at connector CON3. In both cases, the operating field condition shall be verified by monitoring the voltage on the calibration coil.

WARNING — R2 value should be between xx and yy Ω. Check this range at least once before using the alternative method.

d) Position the Reference PICC in any possible PICC position. The d.c. voltage at CON3 shall not exceed 3 V.

6.1.1.3 Test report

The test report shall give the d.c. voltage measured at CON3.

6.2 PICC tests

6.2.1 Alternating magnetic field

The purpose of this test is to check the behaviour of the PICC in relation to alternating magnetic field exposure. Alternating magnetic field shall be tested only at 13,56 MHz. No test is required at other frequencies.

6.2.1.1 Apparatus

The test PCD assembly shall be used to produce the alternating magnetic field.

6.2.1.2 Test procedure

The procedure is as follows.

a) Adjust the RF power delivered by the signal generator to the test PCD antenna to a field strength of 10 A/m (rms) as measured by the calibration coil.

b) Place the PICC under test in the DUT position and readjust immediately the RF drive into the test PCD antenna to the required field strength if necessary.

c) After 5 min, remove the PICC from the DUT position for at least 5 s.

d) Adjust the RF power delivered by the signal generator to the test PCD antenna to a field strength of 12 A/m (rms) as measured by the calibration coil.

e) Place the PICC under test in the DUT position and readjust immediately the RF drive into the test PCD antenna to the required field strength if necessary.

f) Apply for 5 min an ASK 100 % modulation to this field with the following duty cycle:

— 5 s at 0 A/m (rms);

— 25 s at 12 A/m (rms).

g) Check that the PICC operates as intended.

6.2.1.3 Test report

The test report shall state whether or not the PICC operates as intended.

6.2.2 Static electricity test

The purpose of this test is to check the behaviour of the card IC in relation to electrostatic discharge (ESD) exposure in the test sample. The PICC under test is exposed to a simulated electrostatic discharge (ESD, human body model) and its basic operation checked following the exposure..

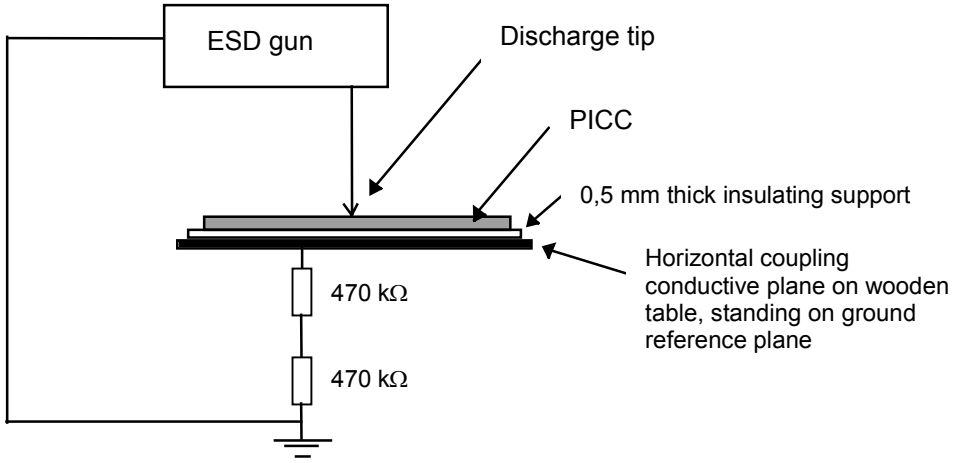


Figure 8 — ESD test circuit

6.2.2.1 Apparatus

Refer to IEC 61000-4-2:1995.

h) Main specifications of the ESD generator:

— energy storage capacitance: 150 pF ± 10 %;

— discharge resistance: 330 Ω ± 10 %;

— charging resistance: between 50 MΩ and 100 MΩ;

— rise time: 0,7 ns to 1 ns.

i) Selected specifications from the optional items:

— type of equipment: table top equipment;

— discharge method: direct application of air discharge to the equipment under test;

— discharge electrodes of the ESD generator: Round tip probe of 8 mm diameter.

6.2.2.2 Test procedure

Connect the ground pin of the apparatus to the conductive plate upon which the PICC is placed.

Apply the discharge successively in normal polarity to each of the 20 test zones shown in Figure 9 — Test zones on PICC for ESD test. Then repeat the same procedure with reversed polarity. Allow a cool-down period between successive pulses of at least 10 s.

WARNING — If the PICC includes contacts, the contacts should face up and the zone which includes contacts should not be exposed to this discharge.

Check that the PICC operates as intended at the end of the test.

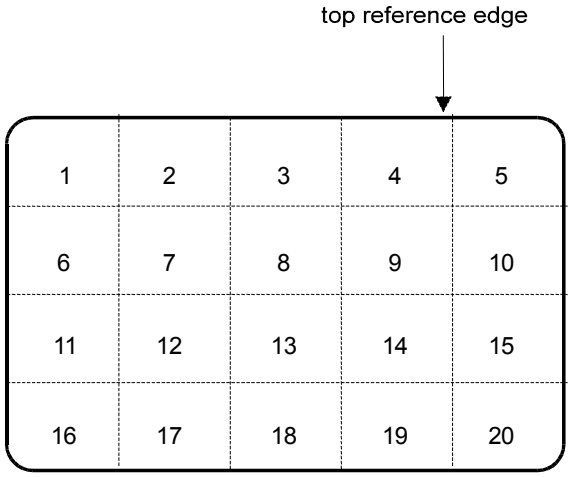


Figure 9 — Test zones on PICC for ESD test

6.2.2.3 Test report

The test report shall state whether or not the PICC operates as intended.

7 Test of ISO/IEC 14443-2 parameters

7.1 PCD tests

All the tests described below will be done in the operating volume as defined by the PCD manufacturer.

7.1.1 PCD field strength

7.1.1.1 Purpose

This test measures the field strength produced by a PCD with its specified antenna in its operating volume as defined in accordance with the base standard.

NOTE The test takes account of PICC loading of the PCD.

7.1.1.2 Test procedure

Procedure for H_{max} test:

a) Tune the Reference PICC to 19 MHz as described in 5.4.5

b) Calibrate the Test PCD assembly to produce the H_{max} operating condition on the calibration coil.

c) Place the Reference PICC into the DUT position on the Test PCD assembly. Switch the jumper J1 to position 'b' and adjust R2 to obtain a d.c. voltage of 3 V measured at connector CON3. Alternatively, jumper J1 may be set to position 'c' and the applied voltage on CON2 is adjusted to obtain a d.c. voltage of 3V at connector CON3. In both cases, the operating field condition shall be verified by monitoring the voltage on the calibration coil.

WARNING — R2 value should be between 75 and 85 Ω. Check this range at least once before using the alternative method.

d) Position the Reference PICC within the defined operating volume of the PCD under test. The d.c. voltage at CON3 shall not exceed 3 V.

Procedure for H_{min} test:

a) Tune the Reference PICC to 13,56 MHz as described in 5.4.5

b) Calibrate the Test PCD assembly to produce the H_{min} operating condition on the calibration coil.

c) Place the Reference PICC into the DUT position on the Test PCD assembly. Switch the jumper J1 to position 'b' and adjust R2 to obtain a d.c. voltage of 3 V measured at connector CON3. Alternatively, jumper J1 may be set to position 'c' and the voltage on CON2 is adjusted to obtain a d.c. voltage of 3V at connector CON3. In both cases, the operating field condition shall be verified by monitoring the voltage on the calibration coil.

WARNING — R2 value should be between 400 and 550 Ω. Check this range at least once before using the alternative method.

d) Position the Reference PICC within the defined operating volume of the PCD under test. The d.c. voltage at CON3 shall exceed 3 V.

7.1.1.3 Test report

The test report shall give the d.c. voltage measured at CON3 for R2 or variable load resistor adjusted to H_{min} and H_{max} field strength under the conditions applied.

7.1.2 PCD field strength supporting operation with "Class 1" PICCs

7.1.2.1 Purpose

The following additional PCD test is necessary for interoperability between PCDs and "Class 1" PICCs. This test is similar to PCD field strength test specified in 7.1.1 but uses a Reference PICC adjusted to apply a higher loading effect.

NOTE The loading effect of "Class 1" PICCs is lower than the loading effect of the Reference PICC used in this test (see "Class 1" PICC maximum loading effect test in 7.2.4). This guarantees that H_{min} is supplied in the "Class 1" PCD operating volume if additionally the "Class 1" PICCs' antenna size and location are similar to the Reference PICC (Annex D) antenna size and location. For PICCs with different antenna size and/or location other classes may be created with, for each class, a corresponding reference PICC.

7.1.2.2 Test procedure

The PCD field strength test defined in 7.1.1, procedure for H_{min} test, shall be repeated with the Reference PICC calibrated to obtain 6 V at CON2 instead of 3 V.

NOTE The Reference PICC calibration used in this test is the same as the calibration defined in 7.1.1.

7.1.2.3 Test report

The test report shall give the d.c. voltage measured at CON3 for R2 or variable load resistor adjusted to H_{min} field strength under the conditions applied.

NOTE The volume in which the d.c. voltage exceeds 6 V defines the “Class 1” operating volume.

7.1.3 Power transfer PCD to PICC

7.1.3.1 Purpose

This test is used to determine that the PCD is able to supply a certain power to a PICC placed anywhere within the defined operating volume.

7.1.3.2 Test procedure

a) Tune the Reference PICC to 19 MHz as described in 5.4.5 and set jumper J1 to position 'a'.

b) Position the Reference PICC within the defined operating volume of the PCD under test. The d.c. voltage at CON3 shall exceed 3 V.

7.1.3.3 Test report

The test report shall give the d.c. voltage at CON3 measured within the defined operating volume under the defined conditions.

7.1.4 Modulation index and waveform

7.1.4.1 Purpose

This test is used to determine the index of modulation of the PCD field as well as the rise and fall times and the overshoot values as defined in ISO/IEC 14443-2.

7.1.4.2 Test procedure

a) Position the calibration coil at an arbitrary position in the defined operating volume, and determine the modulation index and waveform characteristics from the induced voltage on the coil displayed on a suitable oscilloscope.

b) Tune the Reference PICC to 16,5 MHz as described in 5.4.5 and switch the jumper J1 to position 'c'.

c) Place the Reference PICC at a particular position in the PCD operating volume.

d) Apply and adjust a d.c. voltage at CON2 to obtain a d.c. voltage at connector CON3 of 3V at that position.

e) Determine the modulation index and waveform characteristic from the voltage at CON4 displayed with a suitable oscilloscope (requirements see 5.1.1).

f) Repeat steps c) to e) for various positions within the operating volume.

NOTE 1 The selected position of the calibration coil within the operating volume is not expected to affect the results

NOTE 2 The Reference PICC load does not represent the worst case loading effect of a PICC. Higher loading effects may be achieved with resonance frequencies closer to carrier frequency (e.g. 15 MHz).

7.1.4.3 Test report

The test report shall give the measured modulation index of the PCD field, the rise and fall times and overshoot values, within the defined operating volume.

7.1.5 Load modulation reception

7.1.5.1 Purpose

This test shall be used to verify that a PCD correctly detects the load modulation of a PICC which conforms to ISO/IEC 14443-2. It is supposed that the PCD has means to indicate correct reception of the subcarrier produced by a PICC.

7.1.5.2 Test procedure

The Reference PICC and its calibration procedure allow the sensitivity of a PCD to load modulation to be assessed. The Reference PICC does not emulate the loading effect of all types of PICC.

a) Tune the Reference PICC to 13,56 MHz as described in 5.4.5 and switch the jumper J1 to position 'c'.

b) Place the Reference PICC at a particular position in the PCD operating volume.

c) Apply and adjust a d.c. voltage at CON2 to obtain a d.c. voltage at connector CON3 of 3 V at that position.

d) Increase the modulation signal amplitude at CON1 to produce responses until the PCD detects at least 10 of them consecutively.

e) Place the Reference PICC in the DUT position on the Test PCD assembly.

f) Adjust the Test PCD assembly to produce a field strength *H* which gives the same voltage at CON3 and note the corresponding field strength by reading the calibration coil voltage.

g) Measure the Reference PICC load modulation amplitude V_{LMA} as described in 7.2.1 and compare it with the standard limit associated with the noted field strength. This measured V_{LMA} level defines the PCD sensitivity criterion in order to compare with the standard limit to perform these test measurements.

h) Repeat steps b) to g) for various positions within the operating volume.

i) Repeat steps a) to h) with Reference PICC resonance frequencies 15 and 19 MHz.

Any position in which the PCD sensitivity is above the standard limit shall be considered out of the operating volume.

NOTE 1 The test coverage may be expanded by using additional resonance frequencies below 13,56 MHz such as 12 MHz and 10 MHz.

NOTE 2 The PCD sensitivity should be below the standard limit to ensure good reception of the PICC load modulation.

NOTE 3 This test does not check that the PCD reception is independent of the phase of the PICC load modulation. Consequently, it cannot guarantee the correct reception of any PICC compliant with ISO/IEC 14443-2.

7.1.5.3 Test report

The test report shall give the PCD load modulation sensitivity for the tested positions.

7.2 PICC tests

7.2.1 PICC transmission

7.2.1.1 Purpose

The purpose of this test is to determine the load modulation amplitude V_{LMA} of the PICC within the operating field range [H_{min}, H_{max}] as specified in the base standard. Also the functionality of the PICC for Type A and Type B within their corresponding modulation ranges as defined in the base standard shall be determined.

NOTE No load modulation test is required for bit rates of *fc*/64, *fc*/32 and *fc*/16.

7.2.1.2 Test procedure

Step 1: The load modulation test circuit of Figure 9 — Test zones on PICC for ESD test and the Test PCD assembly of Figure 4 — Test PCD assembly are used.

Adjust the RF power delivered by the signal generator to the test PCD antenna to the required field strength as measured by the calibration coil. Connect the output of the load modulation test circuit of Figure 3 — Test set-up (principle) to a digital sampling oscilloscope. The 10 Ω potentiometer P1 shall be trimmed to minimise the residual carrier. This signal shall be at least 40 dB lower than the signal obtained by shorting one sense coil.

WARNING — The PICC load modulation amplitude test should be done by increasing the field strength from 0 A/m, thus checking correct PICC operation starting from H_{min}.

Step 2: The PICC under test shall be placed in the DUT position, concentric with sense coil a**.** The RF drive into the test PCD antenna shall be re-adjusted to the required field strength.

Display a segment of at least two cycles of the waveform of the subcarrier load modulation on the digital sampling oscilloscope and store the sampled data in a file for analysis by a computer software programme (see Annex F).

NOTE Care should be taken to apply a proper synchronization method for low amplitude load modulation.

Fourier transform exactly two subcarrier cycles of the sampled modulation waveform using suitable computer software. Use a discrete Fourier transformation with a scaling such that a pure sinusoidal signal results in its peak magnitude. In order to minimize transient effects, avoid to analyse a subcarrier cycle immediately following a non-modulating period or a phase shift of the subcarrier.

The resulting peak amplitudes of the upper and lower sidebands at *fc* + *fs* and *fc* - *fs* shall be above the value defined in the base standard.

A REQA or a REQB command sequence as defined in ISO/IEC 14443-3 shall be sent by the Test PCD to obtain a signal or load modulation response from the PICC.

The frequency *fcm* of the carrier delivered by the signal generator to the test PCD antenna shall be such that two subcarrier cycles correspond exactly to an integer number of samples. The frequency which fulfils this requirement (with common oscilloscope sampling rates) and which is the closest to the nominal carrier frequency *fc* defined in ISO/IEC 14443-2 is *fcm* = 13,559322 MHz.

The discrete Fourier transformation shall be done at the exact sidebands frequencies generated by the PICC under test, i.e. *fcm* (1 – *fs*/*fc*) and *fcm* (1 + *fs*/*fc*). If the programme given in informative annex F of ISO/IEC 10373-6 is used it shall be modified to replace 13,56 MHz by the exact value of *fcm* during the test.

NOTE 1 In order to limit the worst case measurement error to approximately 5% due to inexact frequencies the following tolerances apply:
- *fcm* = 13,559322 MHz, with a relative tolerance of ± 50 x 10^{-6}
- *fcm* measurement relative error + oscilloscope sampling rate relative error: ± 10 x 10^{-6}
(The oscilloscope sampling rate error may be compensated if the *fcm* measurement is done by the digital sampling oscilloscope. A better than ± 10 x 10^{-6} relative uncertainty may be achieved by sampling more than 500 periods of unmodulated carrier and using interpolation to know precisely the time of the first and of the last rising edge of the carrier.)

NOTE 2 In order to limit the measurement error due to noise (quantization noise, PICC noise…) the following techniques may be used:
- increasing the oscilloscope sampling rate
- increasing the number of subcarrier cycles used in the Fourier transformation

NOTE 3 For Type B PICC load modulation test, the oscilloscope FFT option may also be used on a large number of subcarrier cycles with neither transient effect nor phase shift (i.e. on a stable part of synchronization time TR1 as defined in ISO/IEC 14443-2:2001, 9.2.5 or on a stable part of SOF as defined in ISO/IEC 14443-3:2001, 7.1.4).

7.2.1.3 Test report

The test report shall give the measured peak amplitudes of the upper and lower sidebands at *fc* + *fs* and *fc* - *fs* and the applied fields and modulations.

7.2.2 PICC reception

7.2.2.1 Purpose

The purpose of this test is to verify the ability of the PICC to receive the PCD commands.

7.2.2.2 Conditions for Type A

7.2.2.2.1 Bit rate of *fc*/128

Three test conditions are defined at the border of the Type A PICC modulation waveform timing parameters zone defined in ISO/IEC 14443-2, Figure 4:

— Condition 1: maximum t_1-t_2 and maximum t_3, minimum overshoot

— Condition 2: minimum achievable t_1-t_2 and maximum associated t_3, maximum overshoot

— Condition 3: minimum achievable t_3 and maximum associated t_1-t_2, maximum overshoot

These 3 tests conditions shall be tested at least using *H*min and *H*max.

7.2.2.2.2 Bit rates of *fc*/64, *fc*/32 and *fc*/16

Three test conditions are defined at the border of the Type A PICC modulation waveform timing parameters zone defined in ISO/IEC 14443-2, Figures 7, 8 and 9:

— Condition 1: maximum t_1-t_5 and maximum t_6, minimum overshoot

— Condition 2: minimum achievable t_1-t_5 and maximum associated t_6, maximum overshoot

— Condition 3: minimum achievable t_6 and maximum associated t_1-t_5, maximum overshoot

These 3 tests conditions shall be tested at least using *H*min and *H*max whereas parameter *a* is the maximum specified value when condition 1 is used and is the minimum achievable value for the Test PCD assembly when condition 2 is used.

7.2.2.2.3 Test procedure

Under the conditions defined in 7.2.2.2.1 the PICC shall answer to a REQA with ATQA.

A PICC supporting the optional *fc*/64 bit rate shall operate under the conditions defined in 7.2.2.2.2 after selection of a bit rate of *fc*/64. This PICC shall respond correctly to an I-block transmitted at a bit rate of *fc*/64.

A PICC supporting the optional *fc*/32 bit rate shall operate under the conditions defined in 7.2.2.2.2 after selection of a bit rate of *fc*/32. The PICC shall respond correctly to an I-block transmitted at a bit rate of *fc*/32.

A PICC supporting the optional *fc*/16 bit rate shall operate under the conditions defined in 7.2.2.2.2 after selection of a bit rate of fc/16. The PICC shall respond correctly to an I-block transmitted at a bit rate of *fc*/16.

7.2.2.2.4 Test report

The test report shall confirm the intended operation at the mandatory *fc*/128 bit rate. For PICCs supporting one or more of the optional high bit rates the test report shall confirm the intended operation at the supported bit rates.

7.2.2.3 Conditions for Type B

Three test conditions are defined at the border of the Type B PICC modulation waveform timing parameters zone defined in ISO/IEC 14443-2, Figures 14, 15, 16 and 17:

— Condition 1: maximum t_f and maximum t_r, minimum undershoot and overshoot

— Condition 2: minimum achievable t_f and maximum associated t_r, maximum undershoot and overshoot

— Condition 3: minimum achievable t_r and maximum associated t_f, maximum undershoot and overshoot

These 3 tests conditions shall be tested at least using:

— Hmin and Hmax;

— minimum and maximum modulation index m for the associated field strength applied.

7.2.2.3.1 Test procedure

Under the conditions defined in 7.2.2.3 the PICC operating at a bit rate of *fc*/128 shall answer to a REQB with ATQB.

A PICC supporting the optional *fc*/64 bit rate shall operate under the conditions defined in 7.2.2.3 after selection of a bit rate of *fc*/64. This PICC shall respond correctly to an I-block transmitted at a bit rate of *fc*/64.

A PICC supporting the optional *fc*/32 bit rate shall operate under the conditions defined in 7.2.2.3 after selection of a bit rate of *fc*/32. The PICC shall respond correctly to an I-block transmitted at a bit rate of *fc*/32.

A PICC supporting the optional *fc*/16 bit rate shall operate under the conditions defined in 7.2.2.3 after selection of a bit rate of fc/16. The PICC shall respond correctly to an I-block transmitted at a bit rate of *fc*/16.

7.2.2.3.2 Test report

The test report shall confirm the intended operation at the mandatory *fc*/128 bit rate. For PICCs supporting one or more of the optional high bit rates the test report shall confirm the intended operation at the supported bit rates.

7.2.3 PICC resonance frequency (informative)

7.2.3.1 Purpose

The test may be used to measure the resonance frequency of a PICC.

When two or more PICCs are placed in the same PCD energizing field, the resonance frequency of each PICC decreases.

Care should be taken in designing each PICC resonance frequency.

WARNING — The resonance frequency may depend on the field strength used during the measurement.

7.2.3.2 Procedure

The resonance frequency of a PICC is measured by using an impedance analyser or a network analyser or a LCR-meter connected to a calibration coil. The coil of the PICC should be placed on the calibration coil as close as possible, with the axes of the two coils being congruent. The resonance frequency is that frequency at which the resistive part of the measured complex impedance is at maximum.

7.2.3.3 Test report

The test report shall give the PICC resonance frequency and the measurement conditions.

7.2.4 "Class 1" PICC maximum loading effect

7.2.4.1 Purpose

The following additional PICC test is necessary for interoperability between PCDs and "Class 1" PICCs.

NOTE This test improves interoperability only if the "Class 1" PICCs' antenna size and location are similar to the Reference PICC (Annex D) antenna size and location. For PICCs with different antenna size and/or location other classes may be created with, for each class, a corresponding reference PICC. Next revision of ISO/IEC 14443-1 will include the class(es) definition.

7.2.4.2 Test procedure

The PICC loading effect at H_{min} shall be measured using the test PCD assembly. It shall not exceed the loading effect of the Reference PICC tuned to 13,56 MHz and calibrated to obtain 6 V at CON3 at H_{min}. The procedure of this substitution method is as follows.

a) Tune the Reference PICC to 13,56 MHz as described in 5.4.5.

b) Calibrate the Test PCD assembly to produce the H_{min} operating condition on the calibration coil.

c) Place the Reference PICC into the DUT position on the Test PCD assembly. Switch the jumper J1 to position 'b' and adjust R2 to obtain a d.c. voltage of 6 V measured at connector CON3. Alternatively, jumper J1 may be set to position 'c' and the applied voltage on CON2 is adjusted to obtain a d.c.voltage of 6V at connector CON3. In both cases, the operating field condition shall be verified by monitoring the voltage on the calibration coil.

WARNING — R2 value should be between 900 and 1000 Ω. Check this range at least once before using the alternative method.

d) Remove the Reference PICC.

e) Place the PICC under test into the DUT position on the Test PCD assembly.

f) Measure the field strength H_C monitored by the calibration coil.

The field strength H_C shall be greater than H_{min}.

7.2.4.3 Test report

The test report shall give the value H_C.

8 Test of ISO/IEC 14443-3 and ISO/IEC 14443-4 parameters

8.1 PCD

See Annex H and Annex J.

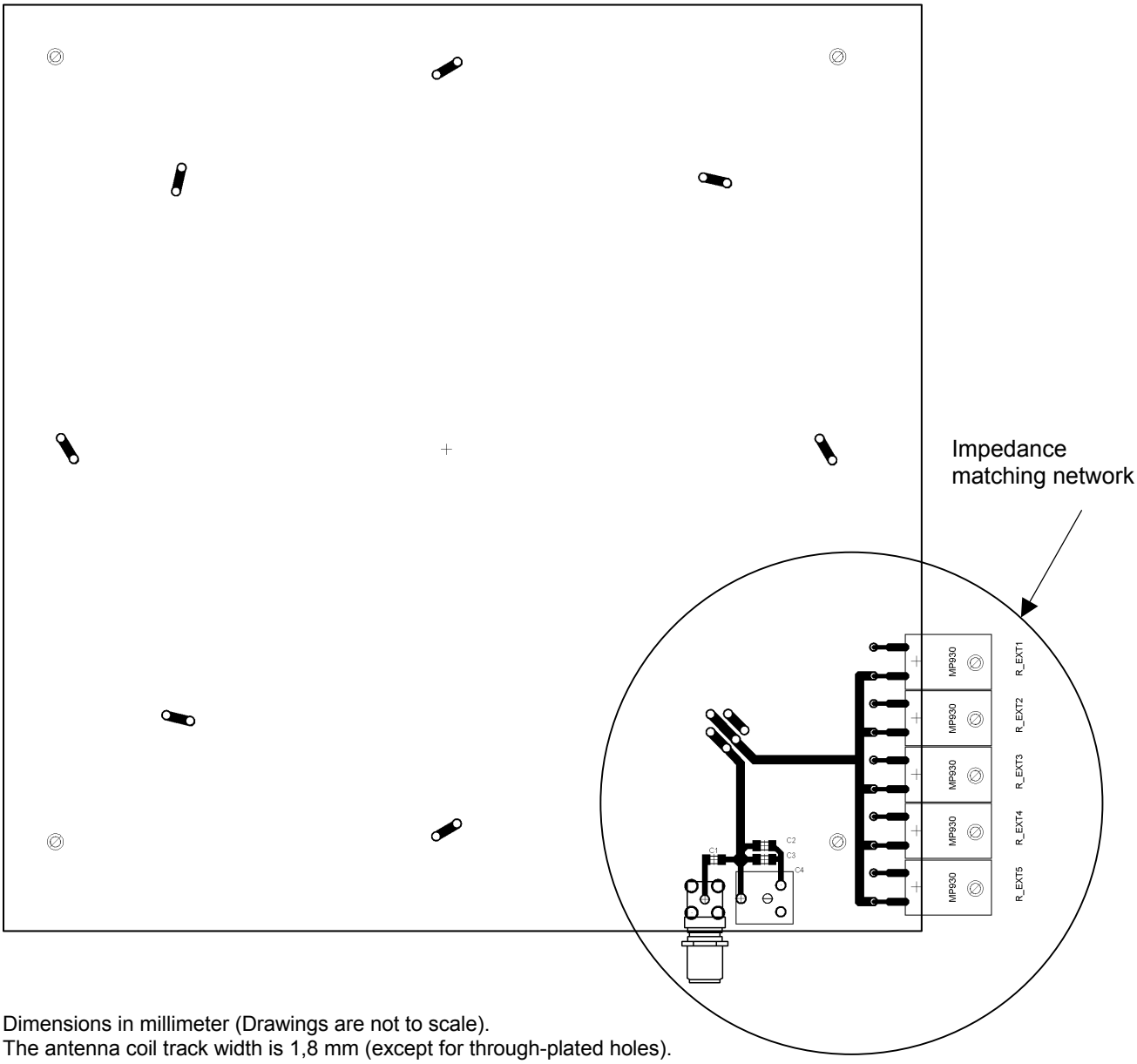
8.2 PICC

See Annex G.

Annex A
(normative)

Test PCD Antenna

A.1 Test PCD Antenna layout including impedance matching network



Dimensions in millimeter (Drawings are not to scale).
The antenna coil track width is 1,8 mm (except for through-plated holes).
Starting from the impedance matching network there are crossovers every 45°.
Printed circuit board (PCB): FR4 material, thickness 1,6 mm, double sided with 35 µm copper.

Figure A.1 — Test PCD antenna layout including impedance matching network for a bit rate of fc/128 (View from front)

NOTE The layout of the impedance matching network is informative.

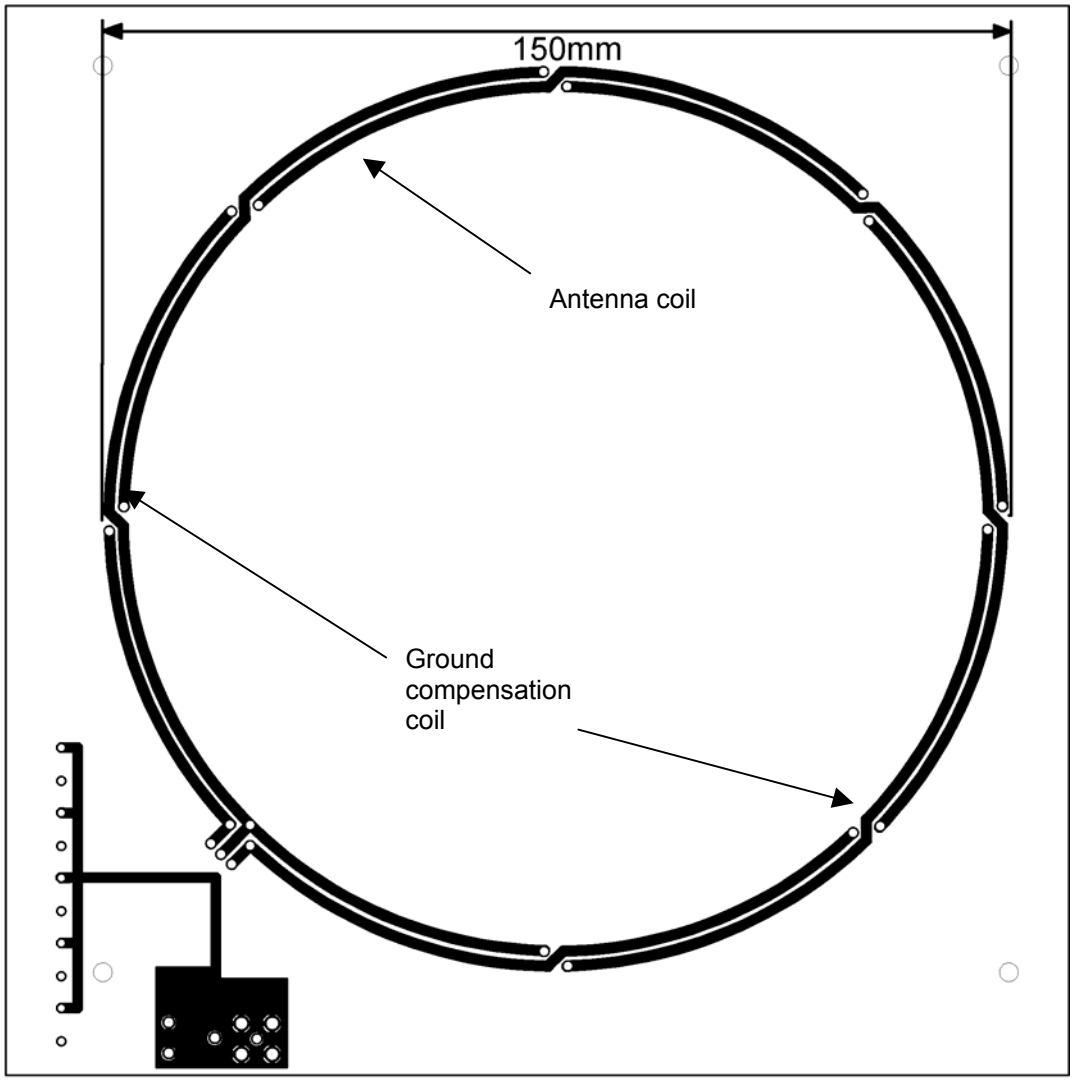
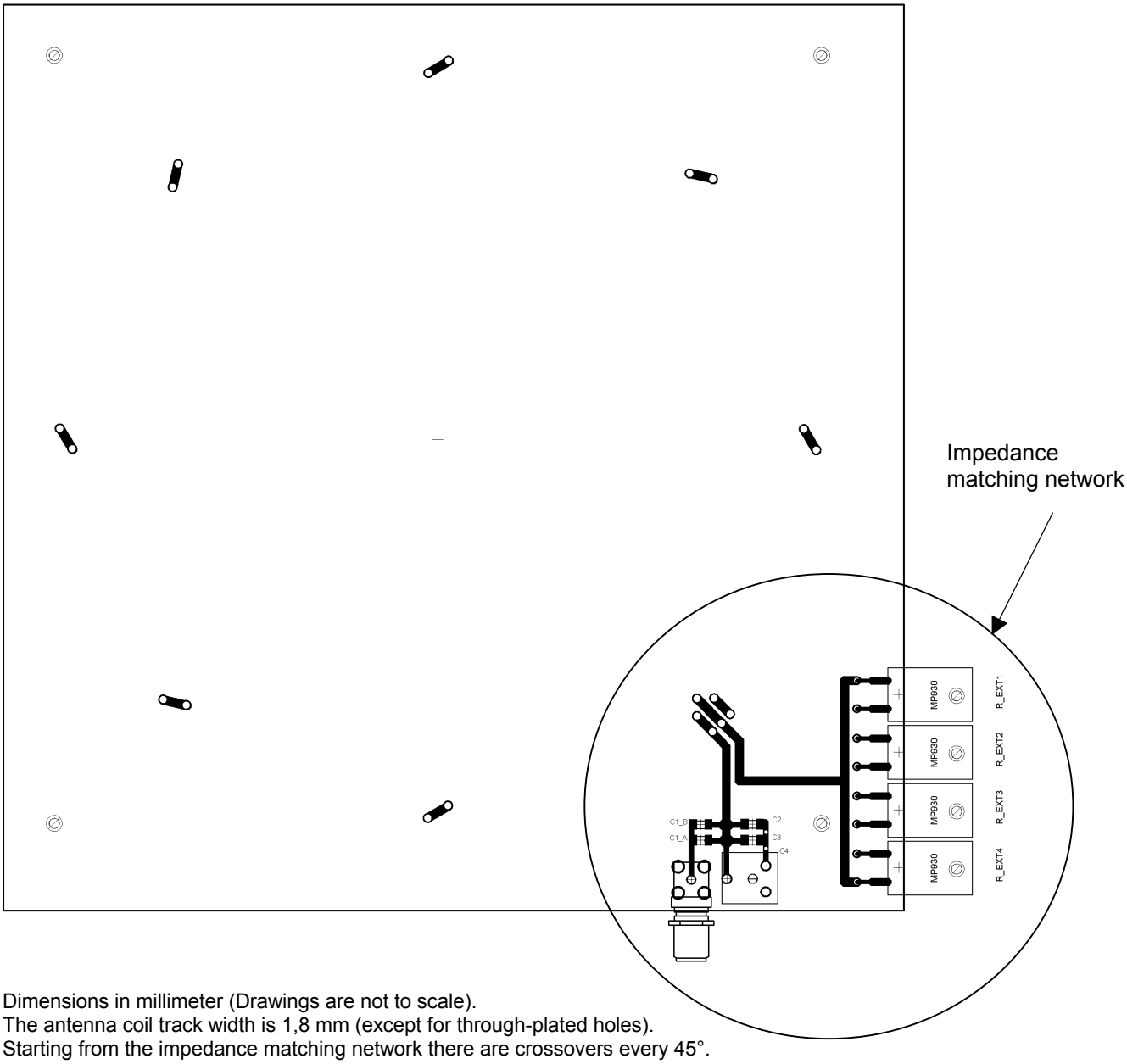


Figure A.2 — Test PCD antenna layout including impedance matching network for a bit rate of fc/128 (View from back)



Dimensions in millimeter (Drawings are not to scale).
The antenna coil track width is 1,8 mm (except for through-plated holes).
Starting from the impedance matching network there are crossovers every 45°.
Printed circuit board (PCB): FR4 material, thickness 1,6 mm, double sided with 35 µm copper.

Figure A.3 — Test PCD antenna layout including impedance matching network for bit rates of fc/64, fc/32 and fc/16 (View from front)

NOTE The layout of the impedance matching network is informative.

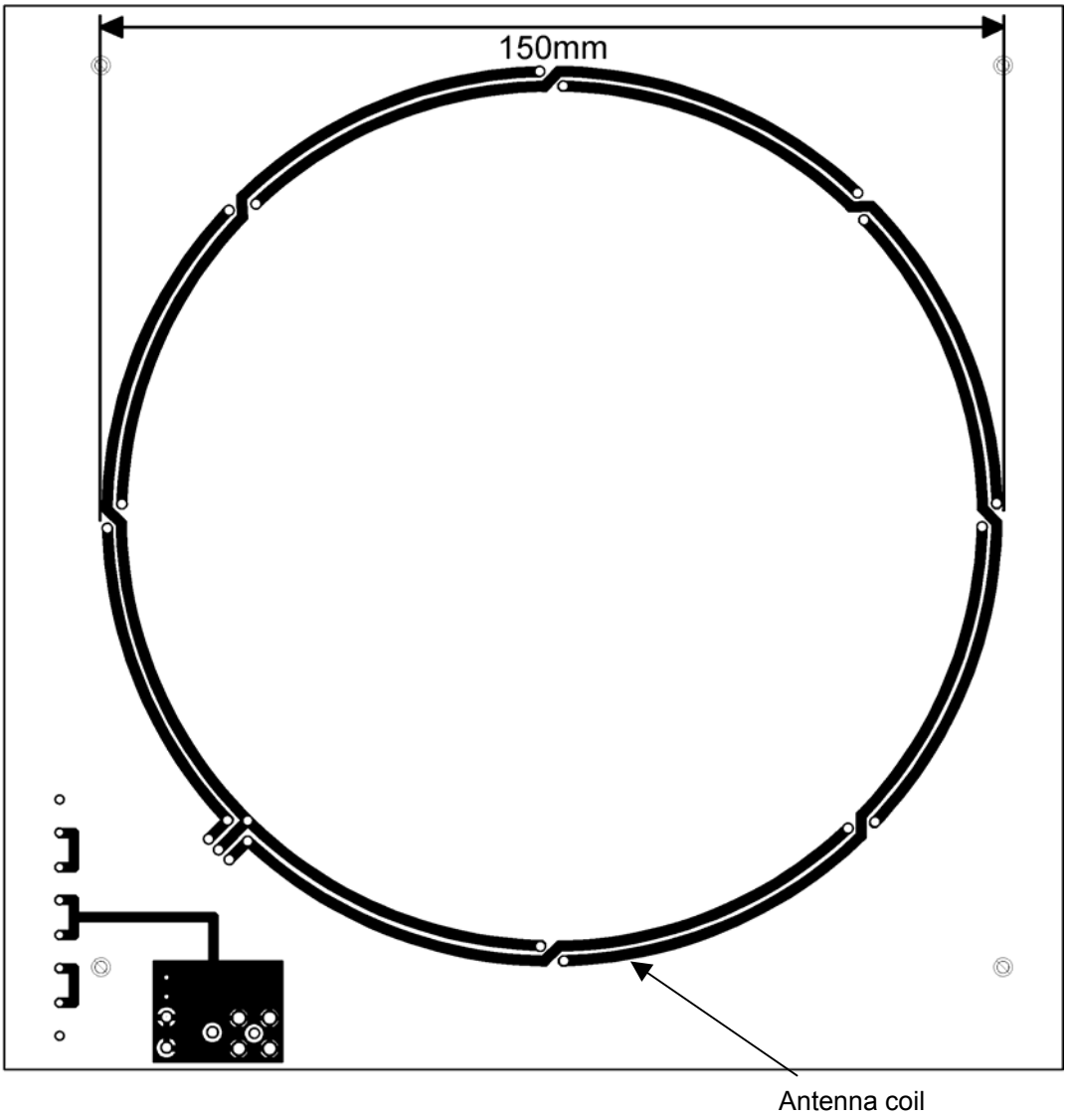


Figure A.4 — Test PCD antenna layout including impedance matching network for bit rates of fc/64, fc/32 and fc/16 (View from back)

NOTE Such printed circuit boards are available from various commercial sources.

A.2 Impedance matching network

The antenna impedance (R_{ant}, L_{ant}) is adapted to the signal generator output impedance (Z = 50Ω) by a matching circuit (see below). The capacitors C1, C2 and C3 have fixed values. The input impedance phase can be adjusted with the variable capacitor C4.

The test PCD assembly as defined in clause 6.2 and in this Annex is intended to be used for time limited measurements, to avoid any overheating of the individual components. If the test is run continuously, heat dissipation shall be improved. Care shall be taken to keep maximum voltages and maximum heat dissipation within the specified limits of the individual components.

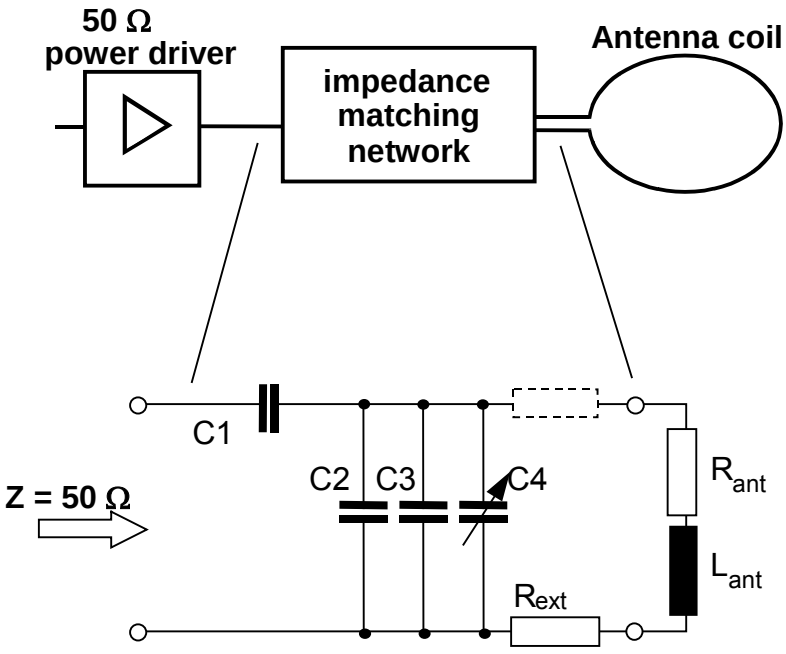
NOTE 1 The tolerance of the matched antenna impedance is +/- 5 Ω and +/- 10°.

NOTE 2 Rext is placed on the ground side of the antenna coil.

NOTE 3 The power and voltage ranges include a safety margin.

NOTE 4 The linear low distortion variable output 50 Ω power driver should be capable of emitting Type A and Type B modulations for transmission of REQ A AND REQ B. For Type B the modulation index should be adjustable in the range of 8% - 14%. The output power should be adjustable to deliver H fields in the range of 1,5 A/m (rms)– 12 A/m (rms). Care should be taken with the duration of fields above the upper operating range of 7,5 A/m (rms).

A.2.1 Impedance matching network for a bit rate of *fc*/128



Component Table:

	Value	Unit	Remarks
C1	47	pF	Voltage range 200V
C2	180	pF	Voltage range 200V
C3	33	pF	Voltage range 200V
C4	2-27	pF	Voltage range 200V
Rext	4,7	Ω	Power range 10 W[a]
[a] 4W with max field of 7.5 A/m (rms)			

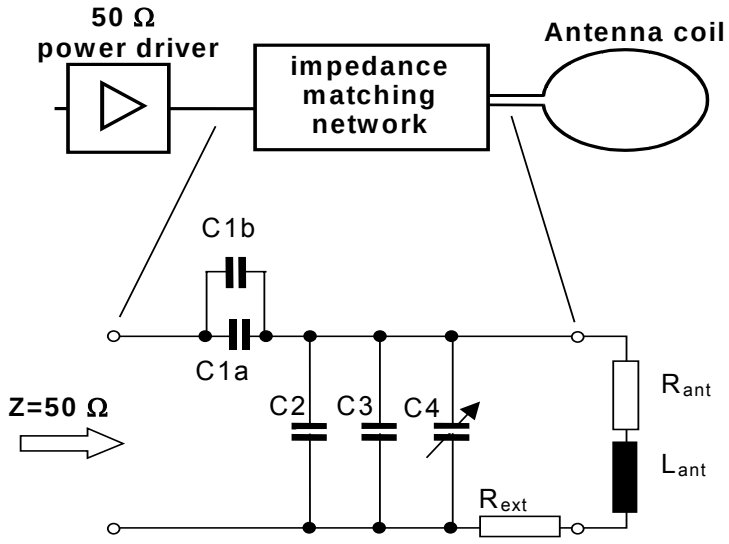
Figure A.3 — Impedance matching network for a bit rate of *fc*/128

NOTE 1 The resistor R_{ext} may be built by connecting five resistors of 4,7 Ω 2W in parallel.

NOTE 2 The resistor R_{ext} may still be placed at the position marked with a dashed outline, as shown in Figure A.3 of ISO/IEC 10373-6:2001.

NOTE 3 Resistor $_{Rext}$ may be 4W if the maximum field is up to 7.5 A/m (rms).

A.2.2 Impedance matching network for bit rates of *fc*/64, *fc*/32 and *fc*/16



Component Table:

	Value	Unit	Remarks
C1a	82	pF	Voltage range 200V
C1b	10	pF	Voltage range 200V
C2	180	pF	Voltage range 200V
C3	10	pF	Voltage range 200V
C4	2-27	pF	Voltage range 200V
Rext	4,7	Ω	Power range 20 W

Figure A.4 — Impedance matching network for bit rates of *fc*/64, *fc*/32 and *fc*/16

NOTE 1 This impedance matching network may also be used for tests for *fc*/128 (although R_{ext} is different).

NOTE 2 This impedance matching network is designed for tests up to 7,5 A/m (rms).

NOTE 3 R_{ext} may be built by 2x2 resistors of 4,7 Ω 5W.

NOTE 4 R_{ext} should be placed on the GND side of the antenna as drawn.

Annex B
(informative)

Test PCD Antenna tuning

The figures below show the two steps of a simple phase tuning procedure to match the impedance of the antenna to that of the driving generator. After the two steps of the tuning procedure the signal generator shall be directly connected to the antenna output for the tests.

Step 1:

A high precision resistor of 50 Ω ± 1% (e.g. 50 Ω BNC resistor) is inserted in the signal line between the signal generator output and an antenna connector. The two probes of the oscilloscope are connected to both sides of the serial reference resistor. The oscilloscope displays a Lissajous figure when it is set in Y to X presentation. The signal generator is set to:

— Wave form: Sinusoidal.

— Frequency: 13,56 MHz.

— Amplitude: 2V (rms) - 5V (rms).

The output is terminated with a second high precision resistor of 50 Ω ± 1% (e.g. 50 Ω BNC terminating resistor). The probe, which is in parallel to the output connector has a small parasitic capacitance C_{probe}. A calibration capacitance C_{cal} in parallel to the reference resistor compensates this probe capacitor if C_{cal} = C_{probe}. The probe capacitor is compensated when the Lissajous figure is completely closed.

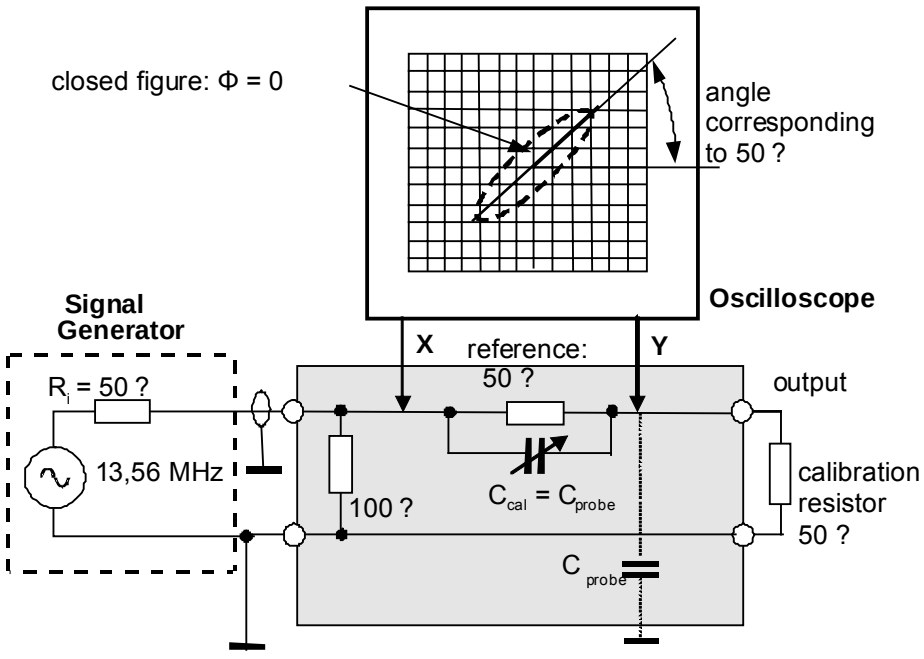


Figure B.1 — Calibration set-up (Step 1)

NOTE The ground cable has to be run close to the probe to avoid induced voltages caused by the magnetic field.

Step 2:

Using the same values as set for step 1, in the second step the matching circuitry is connected to the antenna output. The capacitor C4 on the antenna board is used to tune the phase to zero.

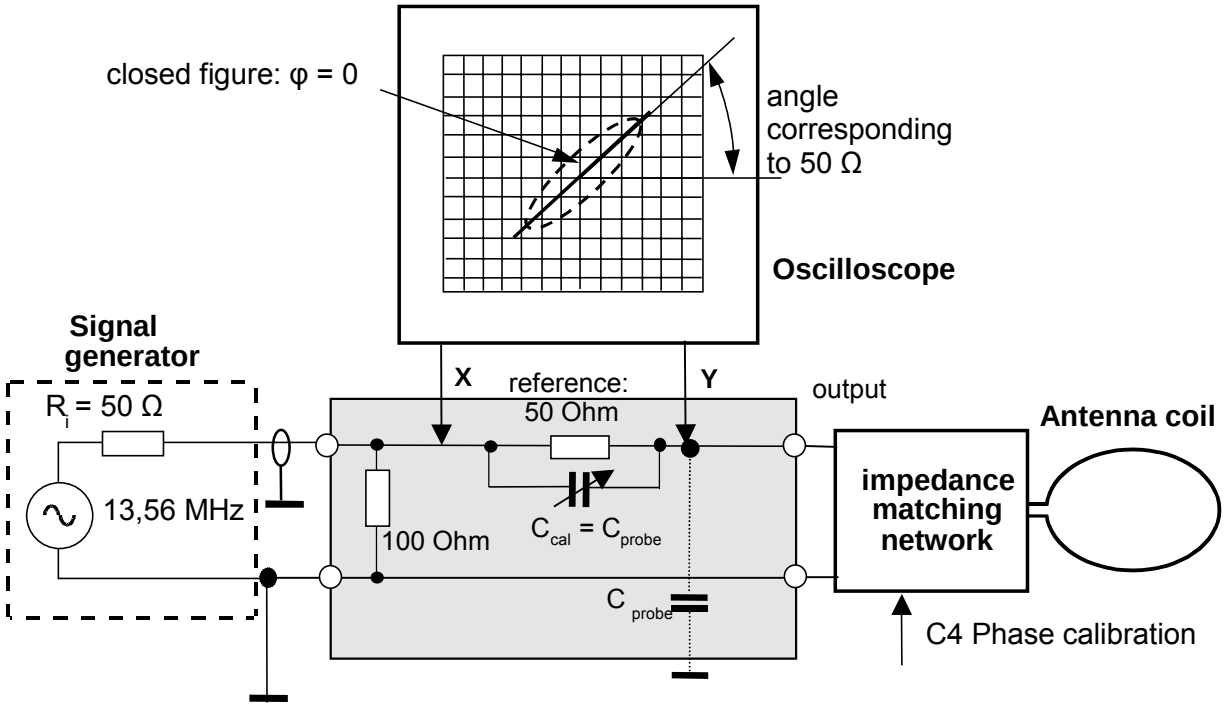
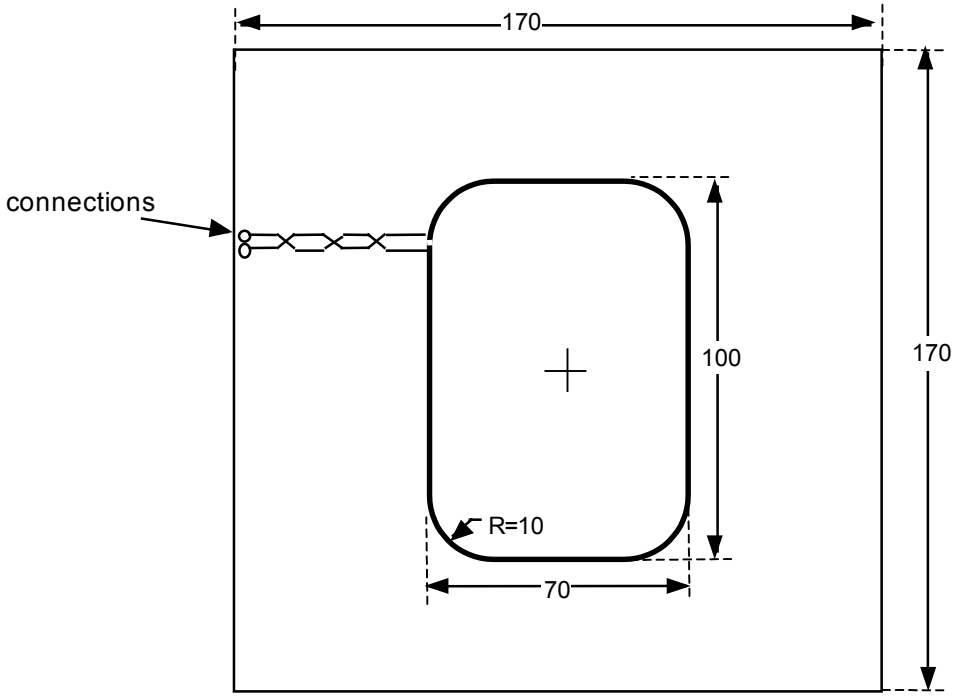


Figure B.2 — Calibration set-up (Step 2)

Annex C
(normative)

Sense coil

C.1 Sense coil layout



Dimensions in millimetres (Drawings are not to scale).
The sense coil track width is 0,5 mm with relative tolerance ± 20 % (except for through-plated holes). Size of the coils refers to the outer dimensions.
Printed circuit board (PCB): FR4 material, thickness 1,6 mm, double sided with 35 µm copper.

NOTE Such printed circuit boards are available from various commercial sources.

Figure C.1 — Layout for sense coils a and b

C.2 Sense coil assembly

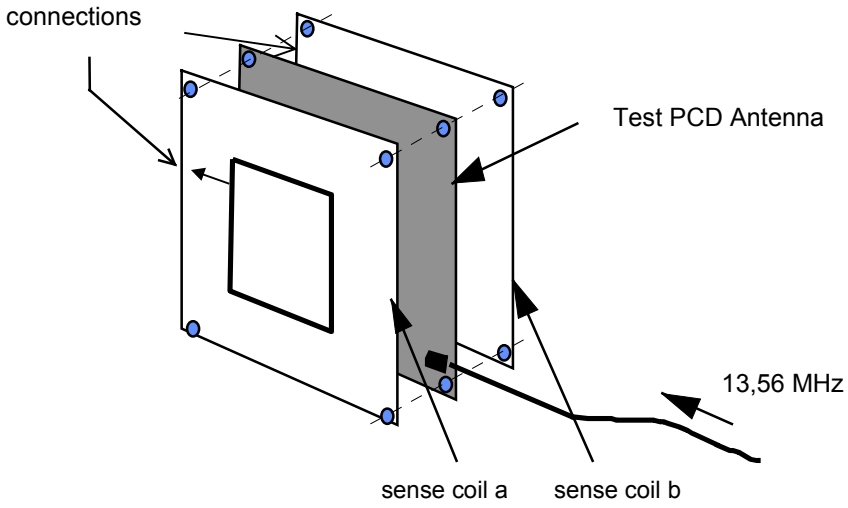
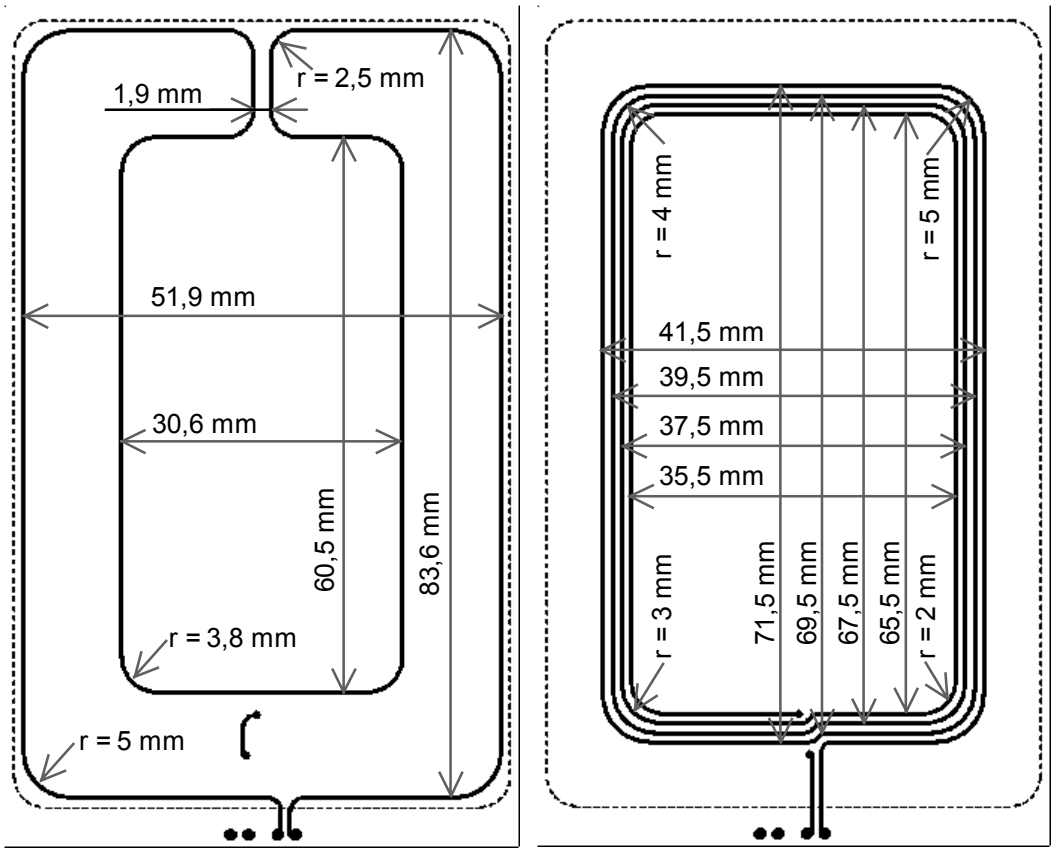


Figure C.2 — Sense coil assembly

Annex D
(normative)

Reference PICC for field and power measurements

D.1 Circuit diagram



(View from front, pick up coil) **(View from back, main coil)**

Figure D.1 — Antenna layout

Dimensions in millimetres to track centre (drawings are not to scale).

The pick up coil and the main coil shall be concentric.

The two coils track width and spacing shall be 0,5 mm with a relative tolerance of ± 20 %.

Printed circuit board (PCB): FR4 material, thickness 0,76 mm with a relative tolerance of ± 10 %, double sided with 35 µm copper.

NOTE Such printed circuit boards are available from various commercial sources.

Annex E
(informative)

Removed

Annex F
(informative)

Program for the evaluation of the spectrum

The following program written in C language gives an example for the calculation of the magnitude of the spectrum from the PICC.

```
/*************************************************************/
/***  This program calculates the fourier coefficients       ***/
/***  of load modulated voltage of a PICC according          ***/
/***  the ISO/IEC 10373-6 Test methods                       ***/
/***  The coefficient are calculated for the frequencies:    ***/
/***    Carrier:        Fcm (=13.5600 for 13.56 MHz)         ***/
/***    Upper sideband: (1+1/16)*Fcm                         ***/
/***    Lower sideband: (1-1/16)*Fcm                         ***/
/*************************************************************/
/*** Input:                                                  ***/
/***  File in CSV Format containing a table of two           ***/
/***  columns (time and test PCD output voltage vd, clause 7)***/
/***                                                         ***/
/***  data format of input-file:                             ***/
/***  -------------------------                              ***/
/***  - one data-point per line:                             ***/
/***     {time[seconds], sense-coil-voltage[volts])          ***/
/***  - contents in ASCII, no headers                        ***/
/***  - data-points shall be equidistant time                ***/
/***  - minimum sampling rate: 100 MSamples/second           ***/
/***  - modulation waveform centred                          ***/
/***      (max. tolerance: half of subcarrier cycle)         ***/
/***                                                         ***/
/***    "screen-shot of centred modulation-waveform          ***/
/***     with 4 subcarrier cycles":                          ***/
/***                                                         ***/
/***   XXXXXXXXXX    xxxx    xxxx    xxxx    xxxxXXXXXXXXXX  ***/
/***   XXXXXXXXXX    xxxx    xxxx    xxxx    xxxxXXXXXXXXXX  ***/
/***   XXXXXXXXXXxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxXXXXXXXXXX  ***/
/***   XXXXXXXXXXxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxXXXXXXXXXX  ***/
/***   XXXXXXXXXXxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxXXXXXXXXXX  ***/
/***   XXXXXXXXXXxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxXXXXXXXXXX  ***/
/***   XXXXXXXXXX    xxxx    xxxx    xxxx    xxxxXXXXXXXXXX  ***/
/***   XXXXXXXXXX    xxxx    xxxx    xxxx    xxxxXXXXXXXXXX  ***/
/***    |-----------------------cc-----------------------|   ***/
/***                                                         ***/
/***  example for spreadsheet file (start in next line):     ***/
/***   (time)      (voltage)                                 ***/
/***  3.00000e-06,1.00                                       ***/
```

```
/***  3.00200e-06,1.01                                          ***/
/***  .....                                                     ***/
/*************************************************************/
/*** RUN:                                                      ***/
/***  Modtst [filename1[.csv] ... filename[.csv] ]             ***/
/*************************************************************/

#include "stdafx.h"
#include <stdio.h>
#include <conio.h>
#include <string.h>
#include <math.h>
#define MAX_SAMPLES 50000
double pi; /* pi=3.14.... */
/* Array for time and sense coil voltage vd */
double vtime[MAX_SAMPLES]; /* time array */
double vd[MAX_SAMPLES]; /* Array for different coil voltage */

/*************************************************************/
/*** Get Carrier Frequency Value Function                  ***/
/***                                                       ***/
/*** Description:                                          ***/
/*** This function Get the carrier frequency value used    ***/
/*** to calculate the DFT                                  ***/
/***                                                       ***/
/*** Input: no input                                       ***/
/***                                                       ***/
/*** Return: Carrier frequency value                       ***/
/*** 0 if an error occurred                                ***/
/***                                                       ***/
/*** Displays Statistics:                                  ***/
/***                                                       ***/
/*** Filename, SampleCount, Sample rate, Max/Min Voltage   ***/
/*************************************************************/
double GetCarrierFrequencyValue(void)
{
  double Fcm=0.0;

  // this function can be replace by a calculation method of the
  // carrier frequency value compute from the acquisition file

  Fcm = 13.56e6F;
  return Fcm;
}

/*************************************************************/
/*** Read CSV File Function                                ***/
/***                                                       ***/
/*** Description:                                          ***/
/*** This function reads the table of time and sense coil  ***/
/*** voltage from a File in CSV Format                     ***/
```

```
/***                                                          ***/
/*** Input: filename                                          ***/
/***                                                          ***/
/*** Return: Number of samples (sample Count)                 ***/
/*** 0 if an error occurred                                   ***/
/***                                                          ***/
/*** Displays Statistics:                                     ***/
/***                                                          ***/
/*** Filename, SampleCount, Sample rate, Max/Min Voltage      ***/
/*************************************************************/
int readcsv(char* fname)
{
  float a,b;
  double max_vd,min_vd;
  int i;
  FILE *sample_file;

/************* Open File ***********************************/
  if (!strchr(fname, '.')) strcat(fname, ".csv");
  if ((sample_file = fopen(fname, "r"))== NULL)
  {
    printf("Cannot open input file %s.\n",fname);
    return 0;
  }
/*************************************************************/
/* Read CSV File */
/*************************************************************/
  max_vd=-1e-9L;
  min_vd=-max_vd;
  i=0;
  while (!feof(sample_file))
  {
    if (i>=MAX_SAMPLES)
    {
      printf("Warning: File truncated !!!\n");
      printf("To much samples in file %s\b\n",fname);
      break;
    }
    fscanf(sample_file,"%f,%f\n", &a, &b);
    vtime[i] = (double)a;
    vd[i] = (double) b;
    if (vd[i]>max_vd) max_vd=vd[i];
    if (vd[i]<min_vd) min_vd=vd[i];
    i++;
  }
  fclose(sample_file);

/************* Displays Statistics ************************/
  printf("\n*********************************************\n");
  printf("\nStatistics: \n");
  printf(" Filename : %s\n",fname);
```

```
  printf(" Sample count: %d\n",i);
  printf(" Sample rate : %1.0f MHz\n",1e-6L/(vtime[1]-vtime[0]));
  printf(" Max(vd) : %4.0f mV\n",max_vd*1000);
  printf(" Min(vd) : %4.0f mV\n",min_vd*1000);
  return i;
}

/*************** End ReadCsv **************/


/*************************************************************/
/*** DFT : Discrete Fourier Transformation                 ***/
/*************************************************************/
/*** Description:                                          ***/
/*** This function calculate the Fourier coefficient       ***/
/***                                                       ***/
/*** Input: Number of samples                              ***/
/*** Global Variables:                                     ***/
/***                                                       ***/
/*** Displays Results:                                     ***/
/***                                                       ***/
/*** Carrier coefficient                                   ***/
/*** Upper sideband coefficient                            ***/
/*** Lower sideband coefficient                            ***/
/***                                                       ***/
/*************************************************************/
void dft(int count)
{
  double c0_real,c0_imag,c0_abs,c0_phase;
  double c1_real,c1_imag,c1_abs,c1_phase;
  double c2_real,c2_imag,c2_abs,c2_phase;
  int N_data,center,start;
  double w0,wu,wl;
  double Wb; //Bartlett window coefficients
  int i,k;

  //add variable for carrier frequency
  double fc;

  //Get the carrier frequency value
  fc=GetCarrierFrequencyValue();


  w0=(double)(fc*2.0)*pi; /* carrier frequency value  MHz          */
  wu=(double)(1.0+1.0/16.0)*w0; /* upper sideband around 14.41 MHz */
  wl=(double)(1.0-1.0/16.0)*w0; /* lower sideband around 12.71 MHz */
  c0_real=0; /* real part of the carrier fourier coefficient       */
  c0_imag=0; /* imag part of the carrier fourier coefficient       */
  c1_real=0; /* real part of the up. sideband fourier coefficient  */
  c1_imag=0; /* imag part of the up. sideband fourier coefficient  */
  c2_real=0; /* real part of the lo. sideband fourier coefficient  */
```

```
  c2_imag=0; /* imag part of the lo. sideband fourier coefficient */
  center=(count+1)/2; /* center address */
/********** signal selection ****************************/

/* Number of samples for Four subcarrier periods          */

  N_data=(int)(0.5+32.0L/(vtime[2]-vtime[1])/fc);
  printf(" N_data: %d\n",N_data);

/* Note: (vtime[2]-vtime[1]) are the scope sample rate    */
  start=center - (int) N_data / 2;

/********************* DFT ******************************/
  for( i=0;i<=N_data-1;i++)
  {
    // Bartlett window
    if ((N_data & 1) == 0)
    {
      //N_data is even
     if (i < (int) N_data /2)
     {
        Wb=2.0L*i/(double)(N_data - 1);
     }
     else
     {
        Wb=2.0L*(N_data-i-1)/(double)(N_data - 1);
     }
    }
    else
    {
      //N_data is odd
      if (i < (int) N_data /2)
      {
        Wb=2.0L*i/(double)(N_data - 1);
      }
      else
      {
        Wb=2.0F-2.0L*i/(double)(N_data - 1);
      }
    }

    k=i+start;
    c0_real=c0_real+vd[k]*(double)cos(w0*vtime[k])*Wb;
    c0_imag=c0_imag+vd[k]*(double)sin(w0*vtime[k])*Wb;
    c1_real=c1_real+vd[k]*(double)cos(wu*vtime[k])*Wb;
    c1_imag=c1_imag+vd[k]*(double)sin(wu*vtime[k])*Wb;
    c2_real=c2_real+vd[k]*(double)cos(wl*vtime[k])*Wb;
    c2_imag=c2_imag+vd[k]*(double)sin(wl*vtime[k])*Wb;
  }
/******************* DFT scale **************************/
    c0_real=4.0F*c0_real/(double) N_data;
```

```
  // 4.0F includes the correction coef. of the bartlett window
  c0_imag=4.0F*c0_imag/(double) N_data;
  c1_real=4.0F*c1_real/(double) N_data;
  c1_imag=4.0F*c1_imag/(double) N_data;
  c2_real=4.0F*c2_real/(double) N_data;
  c2_imag=4.0F*c2_imag/(double) N_data;
  /**************** absolute fourier coefficient **********/
  c0_abs=(double)sqrt(c0_real*c0_real + c0_imag*c0_imag);
  c1_abs=(double)sqrt(c1_real*c1_real + c1_imag*c1_imag);
  c2_abs=(double)sqrt(c2_real*c2_real+c2_imag*c2_imag);
  /************** Phase of fourier coefficient **********/
  c0_phase=(double)atan2(c0_imag,c0_real);
  c1_phase=(double)atan2(c1_imag,c1_real);
  c2_phase=(double)atan2(c2_imag,c2_real);
  /************** Result Display ************************/
  printf("\n\nResults: \n");
  printf("Carrier ");
  printf("Abs: %7.3fmV ",1000*c0_abs);
  printf("Phase: %3.0fdeg\n",c0_phase/pi*180);
  printf("Upper sideband ");
  printf("Abs: %7.3fmV ",1000*c1_abs);
  printf("Phase: %3.0fdeg\n",c1_phase/pi*180);
  printf("Lower sideband ");
  printf("Abs: %7.3fmV ",1000*c2_abs);
  printf("Phase: %3.0fdeg\n\n",c2_phase/pi*180);
  printf("\n*********************************************\n");
  return;
}/**************** End DFT **************/

/*************************************************************/
/*** MAIN Program ***/
/*************************************************************/
int main(unsigned short paramCount,char *paramList[])
{
  char fname[256];
  unsigned int i,sample_count;
  pi = (double)atan(1.0)*4; /* calculate pi */
  printf("\n*********************************************\n");
  printf("\n**** ISO/IEC 10373-6 PICC Test-Program ****\n");
  printf("\n*****      Version: 2.0 APR 2008      *****\n");
  printf("\n*********************************************\n");

/************* No Input Parameter *****************/
  if (paramCount==1)
  {
    printf("\nCSV File name :");
    scanf("%s",fname);
    if (!strchr(fname, '.')) strcat(fname, ".csv");
    if (!(sample_count=readcsv(fname))) return 1;
    dft(sample_count);
  }
```

```
  else
  {
/************* Input Parameter Loop *****************/
  for (i=1;i<paramCount;i++)
  {
    strcpy(fname,paramList[i]);
    if (!strchr(fname, '.')) strcat(fname, ".csv");
    if (!(sample_count=readcsv(fname))) break;
    dft(sample_count);
  }
}

return 0;
}/*********************** End Main ***************************/
```

Annex G
(normative)

Additional PICC test methods

G.1 PICC-test-apparatus and accessories

This clause defines the test apparatus and test circuits for verifying the operation of a PICC according to ISO/IEC 14443-3:2001. The test apparatus includes:

— Calibration coil (see 6.1 of ISO/IEC 10373-6).

— Test PCD assembly (see 6.2 of ISO/IEC 10373-6).

— Digital sampling oscilloscope (see 6.4 of ISO/IEC 10373-6).

Care shall be taken to ensure that the results are not affected by the RF performance of the test circuits.

G.1.1 Emulating the I/O protocol

The PICC-test-apparatus shall be able to emulate the Type A and Type B protocols, which are required to test a PICC.

G.1.2 Generating the I/O character timing in reception mode

The PICC-test-apparatus shall be able to generate the I/O bit stream according to ISO/IEC 14443-3:2001. Timing parameters: start bit length, guard time, bit width, request guard time, start of frame width, end of frame width shall be configurable.

G.1.3 Measuring and monitoring the RF I/O protocol

The PICC-test-apparatus shall be able to measure and monitor the timing of the logical low and high states of the RF Input/Receive line relative to the clock frequency. The PICC-test-apparatus shall be able to monitor the PICC subcarrier.

G.1.4 Protocol Analysis

The PICC-test-apparatus shall be able to analyse the I/O-bit stream in accordance with protocol Type A and Type B as specified in ISO/IEC 14443-3,4 and extract the logical data flow for further protocol analysis.

G.1.5 RFU fields

RFU fields should be constantly monitored during the testing and shall always be verified to contain the assigned default value. A test shall fail and the tested PICC shall be declared non-compliant in case an RFU field is not set to its default value at any time.

G.1.5.1 RFU values

Functional fields should be constantly monitored during the testing and shall always be verified to contain only functional values documented in the standard or proprietary values documented in the standard. A test shall fail and the tested PICC shall be declared non-compliant in case a functional field is not set to said values (and thus is set to an RFU or restricted value) at any time.

G.1.5.2 Timing measurements

The PICC-test-apparatus shall continuously monitor the following frame format and timing values:

For PICC Type A:

— Frame delay time PCD to PICC (see ISO/IEC 14443-3:2001, 6.1.2).

— Frame formats (see ISO/IEC 14443-3:2001, 6.1.5).

— Frame waiting time (see ISO/IEC 14443-4:2001, 7.2).

For PICC Type B:

— Character, frame format and timing (see ISO/IEC 14443-3:2001, 7.1).

— Frame waiting time (see ISO/IEC 14443-4:2001, 7.2).

A test shall fail and the tested PICC be declared non-compliant in case one of the listed timing constraints is violated.

G.1.5.3 Timing measurement report

Fill out Table G.30 — Type A specific timing table for PICC Type A and/or Table G.31 — Type B specific timing table for PICC Type B with the measure timing values

G.2 Relationship of test methods versus base standard requirement

Tests in “Table G.1 — Test methods for logical operation of the PICC Type A protocol” shall apply to Type A PICCs.

Tests in “Table G.2 — Test methods for logical operation of the PICC Type B protocol” shall apply to Type B PICCs.

Tests in “Table G.3 — Test methods for logical operation of PICC of Type A/B” shall apply both to Type A and Type B PICCs.

The ISO/IEC 14443-4:2001 PICC should also comply with ISO/IEC 14443-3:2001 and should be subjected to both the part 3 and part 4 tests for the applicable Type.

A PICC compliant with ISO/IEC 14443-3:2001 but not with ISO/IEC 14443-4:2001 and in ACTIVE or ACTIVE* state (see G.3.3.7, G.3.3.12 and G.4.4.6) may respond with any frame (including Mute) to frames not related to ISO/IEC 14443-3:2001.

Table G.1 — Test methods for logical operation of the PICC Type A protocol

Test method from ISO/IEC 10373-6		Corresponding requirement	
Clause	Name	Base standard	Clause(s)
G.3.2	Polling	ISO/IEC 14443-3:2001	5
G.3.3	Testing of the PICC Type A state transitions	ISO/IEC 14443-3:2001	6.2, 6.3,6.4
G.3.4	Handling of Type A anticollision	ISO/IEC 14443-3:2001	6.3.2
G.3.5	Handling of RATS	ISO/IEC 14443-4:2001	5.6.1
G.3.6	Handling of PPS request	ISO/IEC 14443-4:2001	5.6.2
G.3.7	Handling of FSD	ISO/IEC 14443-4:2001	5.1

Table G.2 — Test methods for logical operation of the PICC Type B protocol

Test method from ISO/IEC 10373-6		Corresponding requirement	
Clause	**Name**	**Base standard**	**Clause(s)**
G.4.2	Polling	ISO/IEC 14443-3:2001	5
G.4.3	PICC Reception	ISO/IEC 14443-3:2001	7.1
G.4.4	Testing of the PICC Type B State Transitions	ISO/IEC 14443-3:2001	7.4 – 7.12
G.4.5	Handling of Type B anticollision	ISO/IEC 14443-3:2001	7.4 – 7.12
G.4.6	Handling of ATTRIB	ISO/IEC 14443-3:2001	7.10
G.4.7	Scenario G.31 Handling of Maximum Frame Size	ISO/IEC 14443-3:2001	7.10.4

Table G.3 — Test methods for logical operation of PICC of Type A/B

Test method from ISO/IEC 10373-6		Corresponding requirement	
Clause	Name	Base standard	Clause(s)
G.5.2	PICC reaction to ISO/IEC 14443-4 Scenarios	ISO/IEC 14443-4:2001	7
G.5.3	Handling of PICC error detection	ISO/IEC 14443-4:2001	7
G.5.4	PICC reaction on CID	ISO/IEC 14443-4:2001	7.1.1.2
G.5.5	PICC reaction on NAD	ISO/IEC 14443-4:2001	7.1.1.3

G.3 Test method for initialisation of the PICC of Type A

G.3.1 Introduction

The tests in this chapter determine whether a PICC of Type A conforms to the ISO/IEC 14443-3 standard and the activation sequence of ISO/IEC 14443-4:2001, 5.

G.3.2 Scenario G.1: Polling

G.3.2.1 Scope

This test is to determine the behaviour of the PICC Type A on receiving REQA commands according to ISO/IEC 14443-3:2001, 5.

G.3.2.2 Procedure

Perform the following steps for 3 different operating fields of 1,5, 4,5 and 7,5 A/m (rms):

a) Place the PICC into the field and adjust it.

b) Switch the RF operating field off for a minimum time for resetting a PICC (see ISO/IEC 14443-3:2001/Amd.1, 5.4).

c) Switch the RF operating field on.

d) Do delay of 5 ms and send a valid REQA Command frame.

e) Record the presence and the content of the PICC response.

f) Switch the RF operating field off for a minimum time for resetting a PICC (see ISO/IEC14443-3:2001/Amd.1, 5.4).

g) Switch the RF operating field on.

h) Wait 5 ms and send a valid REQB Command frame (using Type B modulation and bit coding).

i) Wait 5 ms and send a valid REQA Command frame.

j) Record the presence and the content of the PICC response.

G.3.2.3 Test report

Fill the appropriate row in Table G.32 — Reported Results for Type A specific test methods according to the test results as follows:

Explanation	Test result
Only when the PICC's response is a valid ATQA in both steps 5 and 10	Pass
If the PICC's response isn't a valid ATQA in any of steps 5 or 10	Fail

G.3.3 Testing of the PICC Type A state transitions

G.3.3.1 Scope

These tests verify the correct implementation of the PICC Type A state machine as described in ISO/IEC 14443-3:2001, 6.2.

G.3.3.2 General test outline

For an exhaustive test of the PICC Type A state machine the correctness of every possible state transition at every state shall be verified. Verifying a specific state using a specific state transition will be done as follows:

First, reset the PICC and place it in the test initial state (TIS). This is one of the states from StateSet where the transitions (T) have to be verified. Then execute a transition (T) from TransitionSet. After execution of the state transition, check if the PICC is in the expected target state TTS. There is a difficulty in how to perform this check, because it is impossible to directly inspect the state machine of the PICC. The solution to this problem is to make some additional state transitions and checking the answer of the PICC. The transitions for this purpose are selected in such way that the state can be determined from the PICC answers as precisely as possible.

G.3.3.2.1 Functions for putting the PICC in the Test Initial State (TIS)

Putting the PICC into the State TIS will be done by a sequence of transition commands specified in the following table. The general method is as follows:

In order to put the PICC into State TIS, lookup the corresponding state transition sequence in Table G.4 — State Transition Sequence Table. Then successively apply the state transitions described in the State Transition Sequence column by looking up the corresponding commands in Table G.5 — State Transition Table. Always check the content and integrity of the PICC response.

Table G.4 — State Transition Sequence Table

TIS	State Transition Sequence
POWER-OFF	---
IDLE	POWER-OFF →IDLE

READY(1)	POWER-OFF →IDLE → READY(1)
READY(2)	POWER-OFF →IDLE → READY(1) → READY(2)
READY(3)	POWER-OFF →IDLE → READY(1) → READY(2) → READY(3)
ACTIVE	POWER-OFF →IDLE→ READY(1) → … → READY(CascadeLevels)→ ACTIVE
PROTOCOL	POWER-OFF →IDLE→ READY(1) → … → READY(CascadeLevels) → ACTIVE → PROTOCOL
HALT	POWER-OFF →IDLE → READY(1) → …→ READY(CascadeLevels) → ACTIVE → HALT
READY*(1)	POWER-OFF →IDLE→ READY(1) → … → READY(CascadeLevels) → ACTIVE → HALT → READY*(1)
READY*(2)	POWER-OFF →IDLE → READY(1) → … → READY(CascadeLevels) → ACTIVE → HALT → READY*(1) → READY*(2)
READY*(3)	POWER-OFF →IDLE → READY(1) → … → READY(CascadeLevels) → ACTIVE → HALT → READY*(1) → READY*(2) → READY*(3)
ACTIVE*	POWER-OFF →IDLE → READY(1) → …→ READY (CascadeLevels)→ ACTIVE → HALT → READY*(1) → …→ READY*(CascadeLevels) → ACTIVE*

Table G.5 — State Transition Table

State → Next State	**PICC-test-apparatus**		**PICC**
POWER-OFF → IDLE	Power On (RF Field on)	⟶	
		⟵	Mute
IDLE → READY(1)	REQA	⟶	
		⟵	ATQA
READY(1) → READY(2)	SELECT(1)[a]	⟶	
		⟵	SAK (cascade)
READY(2) → READY(3)	SELECT(2)[a]	⟶	
		⟵	SAK (cascade)
READY(CascadeLevels) → ACTIVE	SELECT (CascadeLevels)[a]	⟶	
		⟵	SAK (complete)
ACTIVE → PROTOCOL	RATS(0,0)	⟶	
		⟵	ATS
ACTIVE → HALT	HLTA	⟶	
		⟵	Mute
HALT→ READY*(1)	WUPA	⟶	
		⟵	ATQA
READY*(1) → READY*(2)	SELECT(1)	⟶	
		⟵	SAK (cascade)
READY*(2) → READY*(3)	SELECT(2)	⟶	
		⟵	SAK(cascade)
READY*(CascadeLevels) →ACTIVE*	SELECT (CascadeLevels)	⟶	
		⟵	SAK (complete)
[a] Any SELECT command may be preceded with an anticollision command to retrieve the PICC UID, especially for random UID.			

G.3.3.2.2 Functions for checking the validity of the test target state TTS

The following table describes the state transitions, which are used to check whether the PICC is in the state S. The content of the PICC answer (i.e. ATQA, SAK ...) should be thoroughly checked for ISO/IEC 14443-3 and ISO/IEC 14443-4 conformance. Please note, that these tests may cause the PICC to change state.

The READY(n)/ READY*(n) states and the ACTIVE/ACTIVE* states cannot be distinguished with one test run. In order to distinguish the "*"-states from the non-"*"-states perform the following steps:

a) Rerun the test a second time, without checking the TTS.

b) Send REQA command. The PICC response shall be Mute.

c) Send REQA command.

d) If the PICC response is Mute then the PICC state was a "*"-state.

e) Else the PICC was a non-"*"-state.

f) The HALT state cannot be distinguished from READY*(n) state and from ACTIVE* state with one test run. In order to distinguish the HALT state perform the following steps:

g) Rerun the test a second time, without checking the TTS.

h) Send WUPA command. The PICC response shall be ATQA.

Table G.6 — Checking the TTS

State S	PICC-test-apparatus		PICC
IDLE	REQA	→	
		←	ATQA
READY(n), n < CascadeLevels	SELECT(n) [a]	→	
		←	SAK (cascade)
READY(n), n = CascadeLevels	SELECT(n) [a]	→	
		←	SAK (complete)
ACTIVE	RATS (0,0)	→	
		←	ATS
PROTOCOL	$I(0)_0$(TEST_COMMAND1(1))	→	
		←	$I(0)_0$(TEST_RESPONSE1(1))
HALT	REQA	→	
		←	Mute
	WUPA	→	
		←	ATQA
READY*(n), n < CascadeLevels	SELECT (n)	→	
		←	SAK (cascade)
READY*(n),	SELECT (n)	→	

State S n = CascadeLevels	PICC-test-apparatus		PICC
		⟵	SAK (complete)
ACTIVE*	RATS(0,0)	⟶	
		⟵	ATS
[a] Any SELECT command may be preceded with an anticollision command to retrieve the PICC UID, especially for random UID.			

G.3.3.3 Scenario G.2: Behaviour of the PICC Type A in the IDLE state

G.3.3.3.1 Scope

This test is to determine the behaviour of the PICC Type A in the IDLE state according to ISO/IEC 14443-3:2001, 6.2.2.

G.3.3.3.2 Procedure

Perform the following steps for every row of Table G.7 — Transitions from IDLE state:

1: Put the PICC into IDLE state.

2: Perform the state transition by sending the command as indicated in the PICC-test-apparatus column.

3: Check if the PICC response is as indicated in the PICC column.

4: If the PICC response is not Mute, check that the Frame Delay Time of the PICC conforms with the value indicated in the FDT column.

5: Check if the PICC is in the state TTS.

Table G.7 — Transitions from IDLE state

Transition	PICC-test-apparatus		PICC	FDT	TTS
REQA	REQA	⟶		1172/*fc*	READY(1)
		⟵	ATQA		
WUPA	WUPA	⟶		1236/*fc*	READY(1)
		⟵	ATQA		
HLTA	HLTA	⟶			IDLE
		⟵	Mute		
AC[c]	('93' NVB $UIDTX_1$[[1..n_1]]) [a]	⟶			IDLE
		⟵	Mute		
nAC[d]	('93' NVB ~$UIDTX_1$[[1.. n_1]]) [a]	⟶			IDLE
		⟵	Mute		
SELECT[c]	SELECT(1)	⟶			IDLE
		⟵	Mute		
nSELECT[d]	('93 70' ~$UIDTX_1$[[1..32]] BCC CRC_A)	⟶			IDLE
		⟵	Mute		
RATS	RATS(0,0)	⟶			IDLE

Transition	PICC-test-apparatus		PICC	FDT	TTS
		⟵	Mute		
PPS	PPS(0,0,0)	⟶			IDLE
		⟵	Mute		
ISO/IEC 14443-4 command	$I(0)_0$(TEST_COMMAND1(1))	⟶			IDLE
		⟵	Mute		
DESELECT	S(DESELECT)	⟶			IDLE
		⟵	Mute		
Error condition	('26') [b]	⟶			IDLE
		⟵	Mute		

[a] Let $1 \leq n_1 \leq 32$.

[b] The value is sent in a standard frame and not in a short frame.

[c] This test is skipped for PICCs exploiting random UID.

[d] For PICCs exploiting a random UID perform this test with a fixed arbitrary UID.

G.3.3.3.3 Test report

Fill the appropriate row in Table G.32 — Reported Results for Type A specific test methods according to the test results as follows:

Explanation	**Test result**
Only when the PICC responded as indicated in the procedure	Pass
Any other case	Fail

G.3.3.4 Scenario G.3: Behaviour of the PICC Type A in the READY(1) state

G.3.3.4.1 Scope

This test is to determine the behaviour of the PICC Type A in the READY state on cascade level 1 according to ISO/IEC 14443-3:2001, 6.2.3.

G.3.3.4.2 Procedure

Perform the following steps for all PICCs and every row of Table G.8 — Transitions from READY(1) state:

a) Put the PICC into READY(1) state.

b) Perform the state transition by sending the command as indicated in the PICC-test-apparatus column.

c) Check if the PICC response is as indicated in the PICC column.

d) If the PICC response is not Mute, check that the Frame Delay Time of the PICC conforms with the value indicated in the FDT column.

e) Check if the PICC is in the state TTS.

Table G.8 — Transitions from READY(1) state

Transition	PICC-test-apparatus		PICC	FDT	TTS
REQA	REQA	⟶			IDLE
		⟵	Mute		
WUPA	WUPA	⟶			IDLE
		⟵	Mute		
HLTA	HLTA	⟶			IDLE
		⟵	Mute		
AC[g] (split after $(0)_b$)	('93' NVB $UIDTX_1[[1..n_1]]$) [a]	⟶		1172/*fc*	READY(1)
		⟵	if n_1=32 then (BCC) else ($UIDTX_1[[n_1+1..32]]$ BCC) [a]		
AC[g] (split after $(1)_b$)	('93' NVB $UIDTX_1[[1..n_2]]$) [b]	⟶		1236/*fc*	READY(1)
		⟵	if n_2=32 then (BCC) else ($UIDTX_1[[n_2+1..32]]$ BCC) [b]		
nAC[g] (wrong UID)	('93' NVB ~$UIDTX_1[[1..n_3]]$) [f]	⟶			IDLE
		⟵	Mute		
SELECT[g]	SELECT(1)	⟶		FDT [c]	TTS [e]
		⟵	SAK [d]		
nSELECT[g] (wrong UID)	('93 70' ~$UIDTX_1$ BCC CRC_A)	⟶			IDLE
		⟵	Mute		
Error condition	('93 70' $UIDTX_1$ BCC ~CRC_A)	⟶			IDLE
		⟵	Mute		
ISO/IEC 14443-4 command	$I(0)_0$(TEST_COMMAND1(1))	⟶			IDLE
		⟵	Mute		
DESELECT	S(DESELECT)	⟶			IDLE
		⟵	Mute		
RATS	RATS(0,0)	⟶			IDLE
		⟵	Mute		
PPS	PPS(0,0,0)	⟶			IDLE
		⟵	Mute		

[a] Let $1 \le n_1 \le 32$, $UIDTX_1[[n_1]] = 0$. If such a number does not exist, the test can be skipped.

[b] Let $1 \le n_2 \le 32$, $UIDTX_1[[n_2]] = 1$ If such a number does not exist, the test can be skipped.

[c] FDT is 1172/fc (~86,43 μs) if last bit = (0)b and 1236/fc (~91,15 μs) if last bit = (1)b, (see margin in the base standard).

[d] Cascade bit of SAK shall be zero for single size UID PICCs and one for double and triple size UID PICCs.

[e] Single size UID PICC shall be in ACTIVE state; double and triple size UID PICCs shall be in READY state.

[f] Let $1 \le n_3 \le 32$.

[g] Any AC or SELECT command may be preceeded with an anticollision command to retrieve the PICC UID, especially for random UID.

G.3.3.4.3 Test report

Fill the appropriate row in Table G.32 — Reported Results for Type A specific test methods according to the test results as follows:

Explanation	Test result
Only when the PICC responded as indicated in the procedure	Pass
Any other case	Fail

G.3.3.5 Scenario G.4: Behaviour of the PICC Type A in the READY(2) state

G.3.3.5.1 Scope

This test is to determine the behaviour of the PICC Type A in the READY state on cascade level 2 according to ISO/IEC 14443-3:2001, 6.2.3. This test is only for PICCs with double or triple size UID.

G.3.3.5.2 Procedure

Perform the following steps for all PICCs with double and triple size UID and every row of Table G.9 — Transitions from READY(2) state:

a) Put the PICC into READY(2) state.

b) Perform the state transition by sending the command as indicated in the PICC-test-apparatus column.

c) Check if the PICC response is as indicated in the PICC column.

d) If the PICC response is not Mute, check that the Frame Delay Time of the PICC conforms with the value indicated in the FDT column.

e) Check if the PICC is in the state TTS.

Table G.9 — Transitions from READY(2) state

Transition	PICC-test-apparatus		PICC	FDT	TTS
REQA	REQA	⟶			IDLE
		⟵	Mute		
WUPA	WUPA	⟶			IDLE
		⟵	Mute		
HLTA	HLTA	⟶			IDLE
		⟵	Mute		
AC[g] (split after $(0)_b$)	('95' NVB $UIDTX_2[[1..n_1]]$) [a]	⟶		1172/*fc*	READY(2)
		⟵	if n_1=32 then (BCC) else ($UIDTX_2[[n_1+1..32]]$ BCC) [a]		
AC[g] (split after $(1)_b$)	('95' NVB $UIDTX_2[[1..n_2]]$) [b]	⟶		1236/*fc*	READY(2)
		⟵	if n_2=32 then (BCC) else ($UIDTX_2[[n_2+1..32]]$ BCC) [b]		
nAC[g] (wrong UID)	('95' NVB ~$UIDTX_2[[1..n_3]]$) [f]	⟶			IDLE
		⟵	Mute		
SELECT[g]	SELECT(2)	⟶		FDT [c]	TTS [e]
		⟵	SAK [d]		
nSELECT[g] (wrong UID)	('95 70' ~$UIDTX_2$ BCC CRC_A)	⟶			IDLE
		⟵	Mute		
Error condition	('95 70' $UIDTX_2$ BCC ~CRC_A)	⟶			IDLE
		⟵	Mute		
ISO/IEC 14443-4 command	$I(0)_0$(TEST_COMMAND1(1))	⟶			IDLE
		⟵	Mute		
DESELECT	S(DESELECT)	⟶			IDLE
		⟵	Mute		
RATS	RATS(0,0)	⟶			IDLE
		⟵	Mute		
PPS	PPS(0,0,0)	⟶			IDLE
		⟵	Mute		

Transition	PICC-test-apparatus	PICC	FDT	TTS

a Let $1 \leq n_1 \leq 32$, $UIDTX_2[[n_1]] = 0$. If such a number does not exist, the test can be skipped.

b Let $1 \leq n_2 \leq 32$, $UIDTX_2[[n_2]] = 1$ If such a number does not exist, the test can be skipped.

c FDT is 1172/fc (~86,43 μs) if last bit = (0)b and 1236/fc (~91,15 μs) if last bit = (1)b, (see margin in the base standard).

d Cascade bit of SAK shall be zero for double size UID PICCs and one for triple size UID PICCs.

e Double size UID PICCs shall be in ACTIVE state; triple size UID PICCs shall be in READY state.

f Let $1 \leq n_3 \leq 32$.

g Any AC or SELECT command may be preceded with an anticollision command to retrieve the PICC UID, especially for random UID.

G.3.3.5.3 Test report

Fill the appropriate row in Table G.32 — Reported Results for Type A specific test methods according to the test results as follows:

Explanation	Test result
If the PICC has a single size UID	Not applicable (NA)
When the PICC has a double or triple size UID and only when it responded as indicated in the procedure	Pass
Any other case	Fail

G.3.3.6 Scenario G.5: Behaviour of the PICC Type A in the READY(3) state

G.3.3.6.1 Scope

This test is to determine the behaviour of the PICC Type A in the READY state according to ISO/IEC 14443-3:2001, 6.2.3. This test is only for PICCs with triple size UID.

G.3.3.6.2 Procedure

Perform the following steps for all PICCs with triple size UID and every row of Table G.10 — Transitions from READY(3) state:

a) Put the PICC into READY(3) state.

b) Perform the state transition by sending the command as indicated in the PICC-test-apparatus column.

c) Check if the PICC response is as indicated in the PICC column.

d) If the PICC response is not Mute, check that the Frame Delay Time of the PICC conforms with the value indicated in the FDT column.

e) Check if the PICC is in the state TTS.

Table G.10 — Transitions from READY(3) state

Transitions	PICC-test-apparatus	PICC	FDT	TTS
REQA	REQA	⟶		IDLE

Transitions	PICC-test-apparatus		PICC	FDT	TTS
		⟵	Mute		
WUPA	WUPA	⟶			IDLE
		⟵	Mute		
HLTA	HLTA	⟶			IDLE
		⟵	Mute		
AC[e] (split after $(0)_b$)	('97' NVB $UIDTX_3[[1..n_1]]$) [a]	⟶			
		⟵	if n_1=32 then (BCC) else ($UIDTX_3[[n_1+1..32]]$ BCC) [a]	1172/*fc*	READY(3)
AC[e] (split after $(1)_b$)	('97' NVB $UIDTX_3[[1..n_2]]$) [b]	⟶			
		⟵	if n_2=32 then (BCC) else ($UIDTX_3[[n_2+1..32]]$ BCC) [b]	1236/*fc*	READY(3)
nAC[e] (wrong UID)	('97' NVB ~$UIDTX_3[[1..n_3]]$) [d]	⟶			
		⟵	Mute		IDLE
SELECT[e]	SELECT(3)	⟶			
		⟵	SAK (complete)	FDT [c]	ACTIVE
nSELECT[e] (wrong UID)	('97 70' ~$UIDTX_3$ BCC CRC_A)	⟶			
		⟵	Mute		IDLE
Error condition	('97 70' $UIDTX_3$ BCC ~CRC_A)	⟶			
		⟵	Mute		IDLE
ISO/IEC 14443-4 command	$I(0)_0$(TEST_COMMAND1(1))	⟶			
		⟵	Mute		IDLE
DESELECT	S(DESELECT)	⟶			
		⟵	Mute		IDLE
RATS	RATS(0,0)	⟶			
		⟵	Mute		IDLE
PPS	PPS(0,0,0)	⟶			
		⟵	Mute		IDLE

a Let $1 \le n_1 \le 32$, $UIDTX_3[[n_1]] = 0$. If such a number does not exist, the test can be skipped.

b Let $1 \le n_2 \le 32$, $UIDTX_3[[n_2]] = 1$ If such a number does not exist, the test can be skipped.

c FDT is 1172/fc (~86,43 μs) if last bit = (0)b and 1236/fc (~91,15 μs) if last bit = (1)b, (see margin in the base standard).

d Let $1 \le n_3 \le 32$.

e Any AC or SELECT command may be preceded with an anticollision command to retrieve the PICC UID, especially for random UID..

G.3.3.6.3 Test report

Fill the appropriate row in Table G.32 — Reported Results for Type A specific test methods according to the test results as follows:

Explanation	Test result
If the PICC has a single or double size UID	Not applicable (NA)
When the PICC has a triple size UID and only when it responded as indicated in the procedure	Pass
Any other case	Fail

G.3.3.7 Scenario G.6: Behaviour of the PICC Type A in the ACTIVE state

G.3.3.7.1 Scope

This test is to determine the behaviour of the PICC Type A in the ACTIVE state according to ISO/IEC 14443-3:2001, 6.2.4.

G.3.3.7.2 Procedure

Perform the following steps for every row of Table G.11 — Transitions from ACTIVE state:

a) Put the PICC into ACTIVE state.

b) Perform the state transition by sending the command as indicated in the PICC-test-apparatus column.

c) Check if the PICC response is as indicated in the PICC column.

d) If the PICC response is not Mute, check that the Frame Delay Time of the PICC is as indicated in the FDT column.

e) Check if the PICC is in the state TTS.

Table G.11 — Transitions from ACTIVE state

Transition	PICC-test-apparatus		PICC	FDT	TTS
REQA	REQA	→			IDLE
		←	Mute		
WUPA	WUPA	→			IDLE
		←	Mute		
AC	('93' NVB $UIDTX_1[[1..n_1]]$)[a]	→			IDLE
		←	Mute		
nAC	('93' NVB ~$UIDTX_1[[1..n_1]]$)[a]	→			IDLE
		←	Mute		
HLTA	HLTA	→			HALT
		←	Mute		
SELECT	SELECT(1)	→			IDLE
		←	Mute		

Transition	PICC-test-apparatus		PICC	FDT	TTS
nSELECT	(‘93 70’ ~UIDTX$_1$ BCC CRC_A)	⟶			IDLE
		⟵	Mute		
RATS	RATS(0,0)	⟶		<65536/*fc*	PROTOCOL
		⟵	ATS		
Error condition	('E0 00' ~CRC_A)	⟶			IDLE
		⟵	Mute		
ISO/IEC 14443-4 command	I(0)$_0$(TEST_COMMAND1(1))	⟶			IDLE
		⟵	Mute		
DESELECT	S(DESELECT)	⟶			IDLE
		⟵	Mute		
PPS	PPS(0,0,0)	⟶			IDLE
		⟵	Mute		
[a] Let $1 \leq n_1 \leq 32$.					

G.3.3.7.3 Test report

Fill the appropriate row in Table G.32 — Reported Results for Type A specific test methods according to the test results as follows:

Explanation	Test result
Only when the PICC responded as indicated in the procedure	Pass
Any other case	Fail

G.3.3.8 Scenario G.7: Behaviour of the PICC Type A in the HALT state

G.3.3.8.1 Scope

This test is to determine the behaviour of the PICC Type A in the HALT state according to ISO/IEC 14443-3:2001, 6.2.5.

G.3.3.8.2 Procedure

For every row of Table G.12 — Transitions from HALT perform the following steps:

a) Put the PICC into HALT state.

b) Perform the state transition by sending the command as indicated in the PICC-test-apparatus column.

c) Check if the PICC response is as indicated in the PICC column.

d) If the PICC response is not Mute, check that the Frame Delay Time of the PICC is as indicated in the FDT column.

e) Check if the PICC is in the state TTS.

Table G.12 — Transitions from HALT

Transition	PICC-test-apparatus		PICC	FDT	TTS
REQA	REQA	⟶			HALT
		⟵	Mute		
WUPA	WUPA	⟶		1236/*fc*	READY*(1)
		⟵	ATQA		
HLTA	HLTA	⟶			HALT
		⟵	Mute		
AC	(‘93’ NVB $UIDTX_1[[1..n_1]]$) [a]	⟶			HALT
		⟵	Mute		
nAC	(‘93’ NVB ~$UIDTX_1[[1..n_1]]$) [a]	⟶			HALT
		⟵	Mute		
SELECT	SELECT(1)	⟶			HALT
		⟵	Mute		
nSELECT	(‘93 70’ ~$UIDTX_1$ BCC CRC_A)	⟶			HALT
		⟵	Mute		
RATS	RATS(0,0)	⟶			HALT
		⟵	Mute		
Error condition	(‘52’) in the standard frame	⟶			HALT
		⟵	Mute		
ISO/IEC 14443-4 command	$I(0)_0$(TEST_COMMAND1(1))	⟶			HALT
		⟵	Mute		
DESELECT	S(DESELECT)	⟶			HALT
		⟵	Mute		
PPS	PPS(0,0,0)	⟶			HALT
		⟵	Mute		

[a] Let $1 \leq n_1 \leq 32$.

G.3.3.8.3 Test report

Fill the appropriate row in Table G.32 — Reported Results for Type A specific test methods according to the test results as follows:

Explanation	**Test result**
Only when the PICC responded as indicated in the procedure	Pass
Any other case	Fail

G.3.3.9 Scenario G.8: Behaviour of the PICC Type A in the READY*(1) state

G.3.3.9.1 Scope

This test is to determine the behaviour of the PICC Type A in the READY* state of cascade level 1 according to ISO/IEC 14443-3:2001, 6.2.6.

G.3.3.9.2 Procedure

Perform the following steps for every row of Table G.13 — Transitions from READY*(1) state:

a) Put the PICC into READY*(1) state.

b) Perform the state transition by sending the command as indicated in the PICC-test-apparatus column.

c) Check if the PICC response is as indicated in the PICC column.

d) If the PICC response is not Mute, check that the Frame Delay Time of the PICC conforms with the value indicated in the FDT column.

e) Check that the PICC is in the state TTS.

Table G.13 — Transitions from READY*(1) state

Transition	PICC-test-apparatus		PICC	FDT	TTS
REQA	REQA	→			HALT
		←	Mute		
WUPA	WUPA	→			HALT
		←	Mute		
HLTA	HLTA	→			HALT
		←	Mute		
AC (split after $(0)_b$)	('93' NVB $UIDTX_1[[1..n_1]]$) [a]	→			
		←	if n_1=32 then (BCC) else ($UIDTX_1[[n_1+1..32]]$ BCC) [a]	1172/*fc*	READY*(1)
AC (split after $(1)_b$)	('93' NVB $UIDTX_1[[1..n_2]]$) [b]	→			
		←	if n_2=32 then (BCC) else ($UIDTX_1[[n_2+1..32]]$ BCC) [b]	1236/*fc*	READY*(1)
nAC (wrong UID)	('93' NVB ~$UIDTX_1[[1..n_3]]$) [f]	→			HALT
		←	Mute		
SELECT	SELECT(1)	→			
		←	SAK [d]	FDT [c]	TTS [e]
nSELECT (wrong UID)	('93 70' ~$UIDTX_1$ BCC CRC_A)	→			HALT
		←	Mute		
Error condition	('93 70' $UIDTX_1$ BCC ~CRC_A)	→			HALT
		←	Mute		

Transition	PICC-test-apparatus		PICC	FDT	TTS
ISO/IEC 14443-4 command	$I(0)_0$(TEST_COMMAND1(1))	⟶			HALT
		⟵	Mute		
DESELECT	S(DESELECT)	⟶			HALT
		⟵	Mute		
RATS	RATS(0,0)	⟶			HALT
		⟵	Mute		
PPS	PPS(0,0,0)	⟶			HALT
		⟵	Mute		

a Let $1 \le n_1 \le 32$, $UIDTX_1[[n_1]] = 0$. If such a number does not exist, the test can be skipped.

b Let $1 \le n_2 \le 32$, $UIDTX_1[[n_2]] = 1$ If such a number does not exist, the test can be skipped.

c FDT is 1172/fc (~86,43 μs) if last bit = (0)b and 1236/fc (~91,15 μs) if last bit = (1)b, (see margin in the base standard).

d Cascade bit of SAK shall be zero for single size UID PICCs and one for double and triple size UID PICCs.

e Single size UID PICCs shall be in ACTIVE state; double and triple size UID PICCs should be in READY state.

f Let $1 \le n_3 \le 32$.

G.3.3.9.3 Test report

Fill the appropriate row in Table G.32 — Reported Results for Type A specific test methods according to the test results as follows:

Explanation	**Test result**
Only when the PICC responded as indicated in the procedure	Pass
Any other case	Fail

G.3.3.10 Scenario G.9: Behaviour of the PICC Type A in the READY*(2) state

G.3.3.10.1 Scope

This test is to determine the behaviour of the PICC Type A in the READY* state of cascade level 2 according to ISO/IEC 14443-3:2001, 6.2.6. This test only applies to PICCs with double or triple size UID.

G.3.3.10.2 Procedure

Perform the following steps for every row of Table G.14 — Transitions from READY*(2) state:

a) Put the PICC into READY*(2) state.

b) Perform the state transition by sending the command as indicated in the PICC-test-apparatus column.

c) Check if the PICC response is as indicated in the PICC column.

d) If the PICC response is not Mute, check that the Frame Delay Time of the PICC conforms with the value indicated in the FDT column.

e) Check if the PICC is in the state TTS.

Table G.14 — Transitions from READY*(2) state

Transition	PICC-test-apparatus		PICC	FDT	TTS
REQA	REQA	⟶			HALT
		⟵	Mute		
WUPA	WUPA	⟶			HALT
		⟵	Mute		
HLTA	HLTA	⟶			HALT
		⟵	Mute		
AC (split after $(0)_b$)	('95' NVB $UIDTX_2[[1..n_1]]$) [a]	⟶			
		⟵	if n_1=32 then (BCC) else ($UIDTX_2[[n_1+1..32]]$ BCC) [a]	1172/*fc*	READY*(2)
AC (split after $(1)_b$)	('95' NVB $UIDTX_2[[1..n_2]]$) [b]	⟶			
		⟵	if n_2=32 then (BCC) else ($UIDTX_2[[n_2+1..32]]$ BCC) [b]	1236/*fc*	READY*(2)
nAC (wrong UID)	('95' NVB ~$UIDTX_2[[1..n_3]]$) [f]	⟶			
		⟵	Mute		HALT
SELECT	SELECT(2)	⟶			
		⟵	SAK [d]	FDT [c]	TTS [e]
nSELECT (wrong UID)	('95 70' ~$UIDTX_2$ BCC CRC_A)	⟶			
		⟵	Mute		HALT
Error condition	('95 70' $UIDTX_2$ BCC ~CRC_A)	⟶			
		⟵	Mute		HALT
ISO/IEC 14443-4 command	$I(0)_0$(TEST_COMMAND1(1))	⟶			
		⟵	Mute		HALT
DESELECT	S(DESELECT)	⟶			
		⟵	Mute		HALT
RATS	RATS(0,0)	⟶			
		⟵	Mute		HALT
PPS	PPS(0,0,0)	⟶			
		⟵	Mute		HALT

a Let $1 \le n_1 \le 32$, $UIDTX_2[[n_1]] = 0$. If such a number does not exist, the test can be skipped.

b Let $1 \le n_2 \le 32$, $UIDTX_2[[n_2]] = 1$ If such a number does not exist, the test can be skipped.

c FDT is 1172/fc (~86,43 μs) if last bit = (0)b and 1236/fc (~91,15 μs) if last bit = (1)b, (see margin in the base standard).

d Cascade bit of SAK shall be zero for double size UID PICCs and one for triple size UID PICCs.

e Double size UID PICCs shall be in ACTIVE state; triple size UID PICCs shall be in READY state.

f Let $1 \le n_3 \le 32$.

G.3.3.10.3 Test report

Fill the appropriate row in Table G.32 — Reported Results for Type A specific test methods according to the test results as follows:

Explanation	Test result
If the PICC has a single size UID	Not applicable (NA)
When the PICC has a double or triple size UID and only when if responded as indicated in the procedure	Pass
Any other case	Fail

G.3.3.11 Scenario G.10: Behaviour of the PICC Type A in the READY*(3) state

G.3.3.11.1 Scope

This test is to determine the behaviour of the PICC Type A in the READY* state of cascade level 3 according to ISO/IEC 14443-3:2001, 6.2.6. This test is only for PICCs with triple size UID.

G.3.3.11.2 Procedure

Perform the following steps for every row of Table G.15 — Transitions from READY*(3) state:

a) Put the PICC into READY*(3) state.

b) Perform the state transition by sending the command as indicated in the PICC-test-apparatus column.

c) Check if the PICC response is as indicated in the PICC column.

d) If the PICC response is not Mute, check that the Frame Delay Time of the PICC conforms with the value indicated in the FDT column.

e) Check if the PICC is in the state TTS.

Table G.15 — Transitions from READY*(3) state

Transition	PICC-test-apparatus		PICC	FDT	TTS
REQA	REQA	→			HALT
		←	Mute		
WUPA	WUPA	→			HALT
		←	Mute		
HLTA	HLTA	→			HALT
		←	Mute		
AC (split after $(0)_b$)	('97' NVB $UIDTX_3[[1..n_1]]$) [a]	→			
		←	if n_1=32 then (BCC) else ($UIDTX_3[[n_1+1..32]]$ BCC) [a]	1172/*fc*	READY*(3)

Transition	PICC-test-apparatus		PICC	FDT	TTS
AC (split after $(1)_b$)	('97' NVB $UIDTX_3[[1..n_2]]$) [b]	⟶		1236/*fc*	READY*(3)
		⟵	if n_2=32 then (BCC) else ($UIDTX_3[[n_2+1..32]]$ BCC) [b]		
nAC (wrong UID)	('97' NVB ~$UIDTX_3[[1..n_3]]$) [d]	⟶			HALT
		⟵	Mute		
SELECT	SELECT(3)	⟶		FDT [c]	ACTIVE*
		⟵	SAK (complete)		
nSELECT (wrong UID)	('97 70' ~$UIDTX_3$ BCC CRC_A)	⟶			HALT
		⟵	Mute		
Error condition	('97 70' $UIDTX_3$ BCC ~CRC_A)	⟶			HALT
		⟵	Mute		
ISO/IEC 14443-4 command	$I(0)_0$(TEST_COMMAND1(1))	⟶			HALT
		⟵	Mute		
DESELECT	S(DESELECT)	⟶			HALT
		⟵	Mute		
RATS	RATS(0,0)	⟶			HALT
		⟵	Mute		
PPS	PPS(0,0,0)	⟶			HALT
		⟵	Mute		

[a] Let $1 \le n_1 \le 32$, $UIDTX_3[[n_1]] = 0$. If such a number does not exist, the test can be skipped.

[b] Let $1 \le n_2 \le 32$, $UIDTX_3[[n_2]] = 1$. If such a number does not exist, the test can be skipped.

[c] FDT is 1172/fc (~86,43 μs) if last bit = (0)b and 1236/fc (~91,15 μs) if last bit = (1)b, (see margin in the base standard).

[d] Let $1 \le n_3 \le 32$.

G.3.3.11.3 Test report

Fill the appropriate row in Table G.32 — Reported Results for Type A specific test methods according to the test results as follows:

Explanation	Test result
If the PICC has a single or double size UID	Not applicable (NA)
When the PICC has a triple size UID and only when it responded as indicated in the procedure	Pass
Any other case	Fail

G.3.3.12 Scenario G.11: Behaviour of the PICC Type A in the ACTIVE* state

G.3.3.12.1 Scope

This test is to determine the behaviour of the PICC Type A in the ACTIVE* state according to ISO/IEC 14443-3:2001, 6.2.7.

G.3.3.12.2 Procedure

Perform the following steps for every row of Table G.16 — Transitions from ACTIVE* state:

a) Put the PICC into ACTIVE state.

b) Perform the state transition by sending the command as indicated in the PICC-test-apparatus column.

c) Check if the PICC response is as indicated in the PICC column.

d) If the PICC response is not Mute, check that the Frame Delay Time of the PICC is as indicated in the FDT column.

e) Check if the PICC is in the state TTS.

Table G.16 — Transitions from ACTIVE* state

Transition	PICC-test-apparatus		PICC	FDT	TTS
REQA	REQA	→			HALT
		←	Mute		
WUPA	WUPA	→			HALT
		←	Mute		
HLTA	HLTA	→			HALT
		←	Mute		
AC	('93' NVB $UIDTX_1$[[1..n_1]]) [a]	→			HALT
		←	Mute		
nAC	('93' NVB ~$UIDTX_1$[[1..n_1]]) [a]	→			HALT
		←	Mute		
SELECT	SELECT(1)	→			HALT
		←	Mute		
nSELECT	('93 70' ~$UIDTX_1$ BCC CRC_A)	→			HALT
		←	Mute		
RATS	RATS(0,0)	→			PROTOCOL
		←	ATS	< 65536/*fc*	
Error condition	('E0 00' ~CRC_A)	→			HALT
		←	Mute		
ISO/IEC 14443-4 command	$I(0)_0$(TEST_COMMAND1(1))	→			HALT
		←	Mute		
DESELECT	S(DESELECT)	→			HALT
		←	Mute		
PPS	PPS(0,0,0)	→			HALT

Transition	PICC-test-apparatus		PICC	FDT	TTS
		←	Mute		
[a] Let $1 \leq n_1 \leq 32$.					

G.3.3.12.3 Test report

Fill the appropriate row in Table G.32 — Reported Results for Type A specific test methods according to the test results as follows:

Explanation	Test result
Only when the PICC responded as indicated in the procedure	Pass
Any other case	Fail

G.3.3.13 Scenario G.12: Behaviour of the PICC Type A in the PROTOCOL state

G.3.3.13.1 Scope

This test is to determine the behaviour of the PICC Type A in the **PROTOCOL** state according to ISO/IEC 14443-4:2001. This test shall ensure that the activated PICC does not respond to any anticollision or initialisation command

G.3.3.13.2 Procedure

For every row of Table G.17 — Transitions from PROTOCOL state perform the following steps:

a) Put the PICC into PROTOCOL state.

b) Perform the state transition by sending the command as indicated in the PICC-test-apparatus column.

c) Check if the PICC response is as indicated in the PICC column.

d) If the PICC response is not Mute, check that the Frame Delay Time of the PICC is as indicated in the FDT column.

e) Check if the PICC is in the state TTS.

Table G.17 — Transitions from PROTOCOL state

Transition	PICC-test-apparatus		PICC	FDT	TTS
REQA	REQA	→			PROTOCOL
		←	Mute		
WUPA	WUPA	→			PROTOCOL
		←	Mute		
AC	('93' NVB $UIDTX_1$[[1..n_1]])[a]	→			PROTOCOL
		←	Mute		
nAC	('93' NVB ~$UIDTX_1$[[1..n_1]])[a]	→			PROTOCOL
		←	Mute		
HLTA	HLTA	→			PROTOCOL
		←	Mute		

Transition	PICC-test-apparatus		PICC	FDT	TTS
SELECT	SELECT(1)	⟶			PROTOCOL
		⟵	Mute		
nSELECT	('93 70' ~UIDTX$_1$ BCC CRC_A)	⟶			PROTOCOL
		⟵	Mute		
RATS	RATS(0,0)	⟶			PROTOCOL
		⟵	Mute		
Error condition	S(DESELECT, ~CRC_A)	⟶			PROTOCOL
		⟵	Mute		
DESELECT	S(DESELECT)	⟶		65536/*fc* as specified in 8.1 of 14443-4	HALT
		⟵	S(DESELECT)		
PPS	PPS(0,0,0)	⟶			PROTOCOL
		⟵	Mute, or PPS response[b]		
ISO/IEC 14443-4 command	$I(0)_0$(TEST_COMMAND1(1))	⟶		< FWT	PROTOCOL
		⟵	$I(0)_0$(TEST_ RESPONSE1(1))		

a Let $1 \leq n_1 \leq 32$.

b PPS response is returned if the PICC supports PPS.

G.3.3.13.3 Test report

Fill the appropriate row in Table G.32 — Reported Results for Type A specific test methods according to the test results as follows:

Explanation	Test result
Only when the PICC responded as indicated in the procedure	Pass
Any other case	Fail

G.3.4 Scenario G.13: Handling of Type A anticollision

G.3.4.1 Scope

This test is to perform a full bitwise anticollision loop according to ISO/IEC 14443-3:2001, 6.4.3.

G.3.4.2 Procedure

a) Put the PICC into the field.

b) Put the PICC into READY(1) state.

c) Execute AnticollisionA.

d) Put the PICC into READY*(1) state.

e) Execute AnticollisionA.

Pseudocode: Type A anticollision procedure

```
1  Procedure AnticollisionA
2  // TPDUSend and TPDURecv are PCD specific functions
3  // to send and receive frames
4
5  for c = 1 to CascadeLevels do
6
7    // anticollision over UID bits
8    for p = 1 to 31[a] do
9      // enter desired cascade level
10     if c ≥ 2 then TPDUSend(SELECT(1))
11     if c = 3 then TPDUSend(SELECT(2))
12     // anticollision with matched bit
13     NVB[[1..4]] = (p + 16) mod 8
14     NVB[[5..8]] = (p + 16) div 8
15     TPDUSend (SEL(c) NVB UIDTXc[[1..p]])
16     if TPDURecv() ≠ (UIDTXc[[p+1..32]] BCC) then return FAIL
17     // anticollision with unmatched bit
18     TPDUSend(SEL(c) NVB UIDTXc[[1..p-1]] ~UIDTXc[[p]])
19     if TPDURecv() ≠ Mute then return FAIL
20     // re-enter READY(1) (resp. READY*(1)) state
21     TPDUSend (WUPA)
22   end for
23 end for
24 return PASS
```

[a] The value 31 may change to 32 at the upcoming revision of the standard

G.3.4.3 Test report

Fill the appropriate row in Table G.32 — Reported Results for Type A specific test methods with test result according the following:

Explanation	Test result
Only when each Anticollision Test every procedure has returned PASS	Pass
When even at one Anticollision Test any procedure has returned the value FAIL	Fail

G.3.5 Handling of RATS

G.3.5.1 Scope

This test is to determine the handling of RATS and ATS by the PICC Type A according to ISO/IEC 14443-4:2001, 5.6.1.

G.3.5.2 Procedure

For the scenarios given in G.3.5.4 the following sequence applies:

a) Put the PICC into ACTIVE state.

b) Send the command sequence as described in the PICC-test-apparatus.

c) Check that the response of the PICC conforms to the one given in the PICC column.

d) For Scenario G.14 check that the PICC is in the IDLE state and for Scenario G.15 check that the PICC is in the PROTOCOL state.

G.3.5.3 Test report

Fill the appropriate rows in Table G.32 — Reported Results for Type A specific test methods according to the test results as follows:

Explanation	Test result
Only when the PICC responded as indicated in the procedure	Pass
Any other case	Fail

G.3.5.4 Scenarios

Scenario G.14: RATS after bad RATS

PICC-test-apparatus		PICC
('E0 00' ~CRC_A)	—/→	
	←	Mute
RATS(0)	→	
	←	Mute

Scenario G.15: RATS after RATS

PICC-test-apparatus		PICC
RATS(0,0)	→	
	←	ATS
RATS(0,0)	→	
	←	Mute

G.3.6 Handling of PPS request

G.3.6.1 Scope

This test is to determine the handling of the PPS request by the PICC Type A according to ISO/IEC 14443-4:2001, 5.6.2.2.

G.3.6.2 Procedure

For each scenario under G.3.6.4 perform the following steps:

a) Put the PICC in PROTOCOL state.

b) Send the command as described under the PICC-test-apparatus column in the table below.

c) Check that the response of the PICC conforms to the one given in the PICC column.

d) Check if the PICC is in PROTOCOL state.

G.3.6.3 Test report

Fill the appropriate rows in Table G.32 — Reported Results for Type A specific test methods according to the test results as follows:

Explanation	Test result
Only when the PICC responded as indicated in the procedure	Pass
Any other case	Fail

G.3.6.4 Scenarios

Scenario G.16: PPS without parameter change

PICC-test-apparatus		PICC
PPS(0,0,0)	⟶	
	⟵	Mute or (‘D0’ CRC_A) [a]
a Response depends on whether the PICC supports PPS or not. If the PICC does not support any changeable parameters it may not support the PPS request because the PCD shall not send PPS to such a PICC (see 14443-4:2001, 5, 6th dash)		

Scenario G.17: PPS without PPS1

PICC-test-apparatus		PICC
(‘D0 01’ CRC_A)	⟶	
	⟵	Mute or (‘D0’ CRC_A)[a]
a Response depends on whether the PICC supports PPS or not. If the PICC does not support any changeable parameters it may not support the PPS request because the PCD shall not send PPS to such a PICC (see 14443-4:2001, 5, 6th dash)		

Scenario G.18: PPS after PPS

PICC-test-apparatus		PICC
PPS(0,0,0)	⟶	
	⟵	Mute or ('D0' CRC_A) [a]
PPS(0,0,0)	⟶	
	⟵	Mute
[a] Response depends on whether the PICC supports PPS or not. If the PICC does not support any changeable parameters it may not support the PPS request because the PCD shall not send PPS to such a PICC (see 14443-4:2001, 5, 6th dash)		

Scenario G.19: PPS after unreceived PPS

PICC-test-apparatus		PICC
(‘D0 01' ~CRC_A)	⟶	
	⟵	Mute
PPS(0,0,0)	⟶	
	⟵	Mute

G.3.7 Scenario G.20: Handling of FSD

G.3.7.1 Scope

This test is to determine if the PICC Type A respects the FSD value as negotiated by the RATS according to ISO/IEC 14443-4:2001, 5.1.

G.3.7.2 Procedure

Perform the following steps for each FSDI = 0 to 8:

a) Put the PICC into ACTIVE state.

b) Send the RATS(0, fsdi) command with parameter fsdi as in the particular test.

c) Check that the PICC answer is a valid ATS and that its size is ≤ FSD.

d) Send the I-block $I(0)_0$(TEST_COMMAND2(2)).

e) Check that the size of the I-block sent by the PICC is ≤ FSD.

G.3.7.3 Test report

Fill the appropriate row in Table G.32 — Reported Results for Type A specific test methods according to the test results as follows:

Explanation	Test result
Only when the PICC responded as indicated in the procedure	Pass
Any other case	Fail

G.4 Test method for initialisation of the PICC of Type B

G.4.1 Introduction

This chapter is to test if the PICC of Type B conforms to the ISO/IEC 14443-3:2001 standard.

G.4.2 Scenario G.21: Polling

G.4.2.1 Scope

This test is to determine the behaviour of the PICC Type B on receiving of REQB according to ISO/IEC 14443-3:2001, 5.

G.4.2.2 Procedure

Perform the following steps for 3 different operating fields of 1,5, 4,5 and 7,5 A/m (rms)

a) Place the PICC into the field and adjust it.

b) Switch the RF operating field off for a minimum time for resetting a PICC in accordance with ISO/IEC14443-3:2001/Amd.1, 5.4.

c) Switch the RF operating field on.

d) Wait 5 ms and send a valid REQB(1) Command frame

e) Record the presence and the content of the PICC response.

f) Switch the RF operating field off for a minimum time for resetting a PICC in accordance with ISO/IEC14443-3:2001/Amd.1, 5.4.

g) Switch the RF operating field on.

h) Wait 5 ms and send a valid REQA Command frame (with Type A modulation).

i) Wait 5 ms and send a valid REQB(1) Command frame.

j) Record the presence and the content of the PICC response.

G.4.2.3 Test report

Fill the appropriate row in “Table G.33 — Reported Results for Type B specific test methods” according to the test results as follows:

Explanation	Test result
Only when the PICC’s response is a valid ATQB in both steps 5 and 10	Pass
When the PICC’s response isn't a valid ATQB in any of steps 5 or 10	Fail

G.4.3 Scenario G.22: PICC Reception

G.4.3.1 Scope

This test is to determine the behaviour of a Type B PICC when receiving PCD messages according to ISO/IEC 14443-3:2001, 7.1.1, 7.1.2, 7.1.4 and 7.1.5.

G.4.3.2 Procedure

Perform the following steps for each row of Table G.18 — Type B frame parameters:

a) Place the reference PICC into the field.

b) Set the frame parameters of the PICC-test-apparatus according to Table G.30 — Type A specific timing table.

c) Send a REQB command.

d) Record the presence, content and timing of the PICC response.

e) Check that the frame format of the PICC response conforms to the following:

— The PICC response shall be a valid ATQB.

— The SOF logic 0 timing shall be between 10 and 11 etu.

— The SOF logic 1timing shall be between 2 and 3 etu.

— The EOF logic 0 timing shall be between 10 and 11 etu.

— The TR0 timing shall be in the range $64/fs \leq TR0 \leq 256/fs$.

— The TR1 timing shall be in the range $80/fs \leq TR1 \leq 200/fs$.

— The PICC shall be turn off the subcarrier between 0 and 2 etu after end EOF.

Table G.18 — Type B frame parameters

EGT [μs]	**SOF (logic 0)** [etu]	**SOF (logic 1)** [etu]	**EOF** [etu]
0	10	2	10
57	10	2	10
0	11	2	10
0	10	3	10
0	10	2	11

G.4.3.3 Test report

Fill the appropriate row in "Table G.33 — Reported Results for Type B specific test methods" according to the test results as follows:

Explanation	Test result
Only when the PICC responded as indicated in the procedure	Pass
Any other case	Fail

G.4.4 Testing of the PICC Type B State Transitions

These tests are to verify the correct implementation of the PICC Type B state machine as described in ISO/IEC 14443-3:2001, 7.4.1.

G.4.4.1 General Test Outline

This is the same procedure as described for the PICC Type A (see G.3.3.2).

G.4.4.1.1 Functions to set the PICC in Test Initial State TIS

Putting the PICC into the State TIS will be done by a sequence of transition commands specified in "Table G.20 — State Transition". The general method is as follows:

In order to put the PICC into State TIS, lookup the corresponding State Transition Sequence in "Table G.19 — State Transition Sequence". Then successively apply the state transitions described in this column by looking up the corresponding commands in the State Transition Table. Always check the content and integrity of the PICC response.

Table G.19 — State Transition Sequence

TIS	State Transition Sequence
POWER-OFF	---
IDLE	POWER-OFF →IDLE
READY REQUESTED	POWER-OFF →IDLE → READY REQUESTED
READY DECLARED	POWER-OFF →IDLE → READY DECLARED
PROTOCOL	POWER-OFF →IDLE → READY DECLARED → PROTOCOL
HALT	POWER-OFF →IDLE → READY DECLARED → HALT

Table G.20 — State Transition

State → Next State	PICC-test-apparatus		PICC
POWER-OFF → IDLE	Power On (RF operating Field on)	⟶	
		⟵	Mute
IDLE → READY REQUESTED	REQB(16)	⟶	
		⟵	Mute [a]
IDLE → READY DECLARED	REQB(1)	⟶	
		⟵	ATQB
READY DECLARED → HALT	HLTB	⟶	
		⟵	'00' CRC_B
READY DECLARED → PROTOCOL	ATTRIB(0,0)	⟶	
		⟵	ATA(0)

State → Next State	PICC-test-apparatus	PICC
[a] In case the PICC has selected slot 1, the REQB command shall be reissued until the PICC doesn't answer ATQB.		

G.4.4.1.2 Functions for checking the validity of the Test Target State TTS

The following "Table G.21 — Checking the TTS" describes the state transitions, which are used to check whether the PICC is in the state S. The content of the PICC answer (i.e. ATQB...) should be thoroughly checked for ISO/IEC 14443-3 and ISO/IEC 14443-4 conformance.

NOTE The tests may cause the PICC to change state.

Table G.21 — Checking the TTS

TTS	PICC-test-apparatus		PICC
IDLE	REQB(1)	⟶	
		⟵	ATQB
READY REQUESTED	SLOTMARKER (n) [a]	⟶	
		⟵	ATQB
READY DECLARED	ATTRIB(0,0)	⟶	
		⟵	ATA(0)
PROTOCOL	$I(0)_0$(TEST_COMMAND1(1))	⟶	
		⟵	$I(0)_0$(TEST_RESPONSE1(1))
HALT	REQB(1)	⟶	
		⟵	Mute
	WUPB(1)	⟶	
		⟵	ATQB
[a] Since the selected PICC slot is unknown, the Slot-MARKER command shall be reissued with different slot values until an ATQB is received.			

G.4.4.2 Scenario G.23: Behaviour of the PICC Type B in the IDLE state

G.4.4.2.1 Scope

This test is to determine the behaviour of the PICC Type B in the IDLE state according to ISO/IEC 14443-3:2001, 7.4.4.

G.4.4.2.2 Procedure

Perform the following steps for every row of Table G.22 — Transitions from IDLE state:

a) Put the PICC into IDLE state.

b) Perform the state transition by sending the command as indicated in the PICC-test-apparatus column.

c) Check if the PICC response is as indicated in the PICC column.

d) Check if the PICC is in the state TTS.

Table G.22 — Transitions from IDLE state

Transition	PICC-test-apparatus		PICC	TTS
REQB	REQB(1)	⟶		READY DECLARED
		⟵	ATQB	
WUPB	WUPB(1)	⟶		READY DECLARED
		⟵	ATQB	
REQB (wrong CRC)	('05 00 00' ~CRC_B)	⟶		IDLE
		⟵	Mute	
WUPB (wrong CRC)	('05 00 08' ~CRC_B)	⟶		IDLE
		⟵	Mute	
HLTB [b]	HLTB	⟶		IDLE
		⟵	Mute	
ATTRIB [b]	ATTRIB(0,0)	⟶		IDLE
		⟵	Mute	
Slot-MARKER	SLOTMARKER(n) [a]	⟶		IDLE
		⟵	Mute	
ISO/IEC 14443-4 command	$I(0)_0$(TEST_COMMAND1(1))	⟶		IDLE
		⟵	Mute	
DESELECT	S(DESELECT)	⟶		IDLE
		⟵	Mute	

[a] n shall run through all values $2 \leq n \leq 16$.

[b] For PICCs using random PUPI apply an arbitrary one for this command.

G.4.4.2.3 Test report

Fill the appropriate row in “Table G.33 — Reported Results for Type B specific test methods” according to the test results as follows:

Explanation	Test result
Only when the PICC responded as indicated in the procedure	Pass
Any other case	Fail

G.4.4.3 Scenario G.24: Behaviour of the PICC Type B in the READY REQUESTED sub-state

G.4.4.3.1 Scope

This test is to determine the behaviour of the PICC Type B in the READY REQUESTED sub-state according to ISO/IEC 14443-3:2001, 7.4.5.

G.4.4.3.2 Procedure

Perform the following steps for every row of Table G.23 — Transitions from READY REQUESTED sub-state:

a) Put the PICC into READY REQUESTED sub-state.

b) Perform the state transition by sending the command as indicated in the PICC-test-apparatus column.

c) Check if the PICC response is as indicated in the PICC column.

d) Check if the PICC is in the state TTS.

Table G.23 — Transitions from READY REQUESTED sub-state

Transition	PICC-test-apparatus		PICC	TTS
REQB	REQB(1)	⟶		READY DECLARED
		⟵	ATQB	
WUPB	WUPB(1)	⟶		READY DECLARED
		⟵	ATQB	
REQB (wrong CRC)	('05 00 00' ~CRC_B)	⟶		READY REQUESTED
		⟵	Mute	
WUPB (wrong CRC)	('05 00 08' ~CRC_B)	⟶		READY REQUESTED
		⟵	Mute	
HLTB [b]	HLTB	⟶		READY REQUESTED
		⟵	Mute	
ATTRIB [b]	ATTRIB(0,0)	⟶		READY REQUESTED
		⟵	Mute	
Slot-MARKER	SLOTMARKER(n) [a]	⟶		READY DECLARED
		⟵	ATQB or Mute	
ISO/IEC 14443-4 command	$I(0)_0$(TEST_COMMAND1(1))	⟶		READY REQUESTED
		⟵	Mute	
DESELECT	S(DESELECT)	⟶		READY REQUESTED
		⟵	Mute	

[a] n shall run through all values $2 \leq n \leq 16$. The PICC shall respond ATQB at exactly one value of n, else Mute.

[b] For PICCs using random PUPI apply an arbitrary one for this command.

G.4.4.3.3 Test report

Fill the appropriate row in “Table G.33 — Reported Results for Type B specific test methods” according to the test results as follows:

Explanation	Test result
Only when the PICC responded as indicated in the procedure	Pass
Any other case	Fail

G.4.4.4 Scenario G.25: Behaviour of the PICC Type B in the READY DECLARED sub-state

G.4.4.4.1 Scope

This test is to determine the behaviour of the PICC Type B in the READY DECLARED sub-state according to ISO/IEC 14443-3:2001, 7.4.6.

G.4.4.4.2 Procedure

Perform the following steps for every row of Table G.24 — Transitions from READY DECLARED SUB-state:

a) Put the PICC into READY DECLARED SUB-state.

b) Perform the state transition by sending the command as indicated in the PICC-test-apparatus column.

c) Check if the PICC response is as indicated in the PICC column.

d) Check if the PICC is in the state TTS.

Table G.24 — Transitions from READY DECLARED SUB-state

Transition	PICC-test-apparatus		PICC	TTS
REQB	REQB(1)	⟶		READY DECLARED
		⟵	ATQB	
WUPB	WUPB(1)	⟶		READY DECLARED
		⟵	ATQB	
REQB (wrong CRC)	('05 00 00' ~CRC_B)	⟶		READY DECLARED
		⟵	Mute	
WUPB (wrong CRC)	('05 00 08' ~CRC_B)	⟶		READY DECLARED
		⟵	Mute	
HLTB	HLTB	⟶		HALT
		⟵	('00' CRC_B)	
ATTRIB	ATTRIB(0,0)	⟶		PROTOCOL
		⟵	ATA(0)	
Slot-MARKER	SLOTMARKER(n) [a]	⟶		READY DECLARED
		⟵	Mute	
ISO/IEC 14443-4 command	$I(0)_0$(TEST_COMMAND1(1))	⟶		READY DECLARED
		⟵	Mute	
DESELECT	S(DESELECT)	⟶		READY DECLARED
		⟵	Mute	

[a] n shall run through all values $2 \leq n \leq 16$.

G.4.4.4.3 Test report

Fill the appropriate row in “Table G.33 — Reported Results for Type B specific test methods” according to the test results as follows:

Explanation	Test result
Only when the PICC responded as indicated in the procedure	Pass
Any other case	Fail

G.4.4.5 Scenario G.26: Behaviour of the PICC Type B in the HALT state

G.4.4.5.1 Scope

This test is to determine the behaviour of the PICC Type B in the HALT state according to ISO/IEC 14443-3:2001, 7.4.8.

G.4.4.5.2 Procedure

Perform the following steps for every row of Table G.25 — Transitions from HALT state:

a) Put the PICC into HALT state.

b) Perform the state transition by sending the command as indicated in the PICC-test-apparatus column.

c) Check if the PICC response is as indicated in the PICC column.

d) Check if the PICC is in the state TTS.

Table G.25 — Transitions from HALT state

Transition	PICC-test-apparatus		PICC	TTS
REQB	REQB(1)	→		HALT
		←	Mute	
WUPB	WUPB(1)	→		READY DECLARED
		←	ATQB	
WUPB (wrong CRC)	('05 00 08' ~CRC_B)	→		HALT
		←	Mute	
HLTB	HLTB	→		HALT
		←	Mute	
ATTRIB	ATTRIB(0,0)	→		HALT
		←	Mute	
Slot-MARKER	SLOTMARKER(n) [a]	→		HALT
		←	Mute	
ISO/IEC 14443-4 command	$I(0)_0$(TEST_COMMAND1(1))	→		HALT
		←	Mute	
DESELECT	S(DESELECT)	→		HALT
		←	Mute	

[a] n shall run through all values $2 \leq n \leq 16$.

G.4.4.5.3 Test report

Fill the appropriate row in “Table G.33 — Reported Results for Type B specific test methods” according to the test results as follows:

Explanation	Test result
Only when the PICC responded as indicated in the procedure	Pass
Any other case	Fail

G.4.4.6 Scenario G.27: Behaviour of the PICC Type B in the PROTOCOL state

G.4.4.6.1 Scope

This test is to determine the behaviour of the PICC Type B in the PROTOCOL state according to ISO/IEC 14443-4:2001. This test shall ensure that the activated PICC does not respond to any initialisation command.

G.4.4.6.2 Procedure

Perform the following steps for every row of Table G.26 — Transitions from PROTOCOL state:

a) Put the PICC into PROTOCOL state.

b) Perform the state transition by sending the command as indicated in the PICC-test-apparatus column.

c) Check if the PICC response is as indicated in the PICC column.

d) Check if the PICC is in the state TTS.

Table G.26 — Transitions from PROTOCOL state

Transition	PICC-test-apparatus		PICC	FDT	TTS
REQB	REQB(1)	→			PROTOCOL
		←	Mute		
WUPB	WUPB(1)	→			PROTOCOL
		←	Mute		
REQB (wrong CRC)	('05 00 00' ~CRC_B)	→			PROTOCOL
		←	Mute		
WUPB (wrong CRC)	('05 00 08' ~CRC_B)	→			PROTOCOL
		←	Mute		
HLTB	HLTB	→			PROTOCOL
		←	Mute		
ATTRIB	ATTRIB(0,0)	→			PROTOCOL
		←	Mute		
Slot-MARKER	SLOTMARKER(n) [a]	→			PROTOCOL
		←	Mute		

Transition	PICC-test-apparatus		PICC	FDT	TTS
ISO/IEC 14443-4 command	I(0)0(TEST_COMMAND1(1))	⟶			
		⟵	$I(0)_0$(TEST_RESPONSE1(1))	< FWT	PROTOCOL
DESELECT	S(DESELECT)	⟶			
		⟵	S(DESELECT)		HALT
[a] n shall run through all values $2 \leq n \leq 16$.					

G.4.4.6.3 Test report

Fill the appropriate row in "Table G.33 — Reported Results for Type B specific test methods" according to the test results as follows:

Explanation	Test result
Only when the PICC responded as indicated in the procedure	Pass
Any other case	Fail

G.4.5 Scenario G.28: Handling of Type B anticollision

G.4.5.1 Scope

The purpose of this test is to determine the handling of a PICC Type B anticollision according to ISO/IEC 14443-3:2001, 7.4.1.

The core of this test is the procedure AnticollisionB(N, outparam chi2) which is defined in the pseudo code below. The procedure performs 256 REQB(N) commands and following Slot-MARKER commands and counts how many times each of the N slots has been selected by the PICC. The procedure also checks if the PICC has mapped each REQB(N) request to exactly one slot. If this is not the case the test returns FAIL.

Since Type B anticollision is based on random selection of the slots, statistical methods shall be used for verification. As it is the nature of all statistical tests, this test can fail even in the case the PICC behaves correctly. This failure is called a "Type I error" in statistical terms. This error cannot be completely avoided. Instead, the probability of its occurrence can be controlled by the so called "significance value" α. This means, the smaller α, the less probable the "Type I error". However, this does not mean that one should select α as small as possible. This is because the smaller α is, the more probable is that the test passes a bad PICC (i.e. a PICC that doesn't select the slots with the right probability). In statistical terms this is called a "Type II error". For this reason it is crucial to select an appropriate significance value α.

The PICC shall additionally select each of the N slots with equal probability (i.e. 1/N). In order to verify this, the statistical χ^2-test on all slots shall be performed. The result of this test is the value chi2 which shall be compared against the $\chi^2_{\alpha,N-1}$ quintile.

G.4.5.2 Procedure

Due to the reasons explained above, it shall be the responsibility of the test lab to choose an appropriate significance value α. Also, if one of the statistical tests fails in step e), the test lab may choose to rerun the test for this parameter N, maybe also with another significance level. On the other hand, the test unconditionally fails in case the AnticollisionB procedure returns FAIL (step 4).

Perform the following steps for each value N = 2, 4, 8, 16.

a) Choose a significance level $\alpha \in \{0,1, 0,05, 0,01, 0,005\}$ and lookup from Table G.27 — a-quintile values, the corresponding α and $\chi^2_{\alpha,N-1}$ quintile.

b) Reset the PICC.

c) Execute AnticollisionB(N, chi2).

d) If AnticollisionB returns FAIL, fail the test.

e) If chi2 $\leq \chi^2_{\alpha,S}$ then pass the test Else fail the test.

Table G.27 — a-quintile values

α	$\chi^2_{\alpha,N-1}$			
	$\chi^2_{\alpha,1}$	$\chi^2_{\alpha,3}$	$\chi^2_{\alpha,7}$	$\chi^2_{\alpha,15}$
0.1	2.706	6.251	12.017	22.307
0.05	3.841	7.815	14.067	24.996
0.01	6.635	11.345	18.475	30.578
0.005	7.879	12.838	20.278	32.801

Pseudocode: Type B anticollision procedure

```
1  Procedure AnticollisionB(N, chi2)
2
3    // TPDUSend and TPDURecv are PCD specific functions
4    // to send and receive TPDU frames
5
6    // probability for selecting slot
7    p = 1/N
8
9    // clear slot counters
10   for i from 1 to 2^N do
11     Slots[i] = 0
12   Endfor
13
14   // collect data
15   for i from 1 to 256 do
16     TPDUSend (REQB(N))
17     if TPDURecv() = ATQB then
18       Slots[1] = Slots[1]+1
19     Else
20       for j from 2 to N do
21         TPDUSend (SLOTMARKER(j))
22         if TPDURecv () = ATQB then
23           Slots[j] = Slots[j]+1
```

```
24          endif
25        endfor
26      endif
27    endfor
28
29    // check that exactly
30    // one slot has been selected at each run
31    cnt = 0
32    for i from 1 to N do
33      cnt = cnt + Slots[i]
34    endfor
35    if cnt ≠ 256 then
36      return FAIL
37    endif
38    Chi2 = 0
39    for i from 1 to N do
40      chi2 = chi2 + Slots[i]*Slots[i]
41    endfor
42    chi2 = chi2*N/256 – 256
43 return PASS
```

NOTE Continue with step e) only of PASS is returned in line 43

G.4.5.3 Test report

Fill the appropriate row in “Table G.33 — Reported Results for Type B specific test methods” according to the test results as follows:

Explanation	Test result
Only when every AnticollisionTest procedure has returned PASS	Pass
When any AnticollisionTest procedure has returned the value FAIL	Fail

G.4.6 Handling of ATTRIB

G.4.6.1 Scope

This test is to determine the behaviour of the PICC Type B on ATTRIB command according to ISO/IEC 14443-3:2001, 7.10.

G.4.6.2 Procedure

Perform the following steps for each of Scenario G.29 and Scenario G.30 listed under clause G.4.6.3:

a) Put the PICC into READY DECLARED sub-state.

b) Send the command sequence as described in the PICC-test-apparatus.

c) Check that the response of the PICC conforms with the one given in the PICC column.

d) Check if the PICC is in PROTOCOL state.

G.4.6.3 Scenarios

Scenario G.29: ATTRIB with wrong PUPI

PICC-test-apparatus		PICC
('1D' ~PUPI '00 00 01 00' CRC_B)	⟶	
	⟵	Mute
ATTRIB(0,0)	⟶	
	⟵	ATA(0)

Scenario G.30: ATTRIB after bad ATTRIB

PICC-test-apparatus		PICC
('1D' PUPI '00 00 01 00' ~CRC_B)	⟶	
	⟵	Mute
ATTRIB(0,0)	⟶	
	⟵	ATA(0)

G.4.6.4 Test report

Fill the appropriate row in "Table G.33 — Reported Results for Type B specific test methods" according to the test results as follows:

Explanation	Test result
Only when the PICC responded as indicated in the procedure	Pass
Any other case	Fail

G.4.7 Scenario G.31 Handling of Maximum Frame Size

G.4.7.1 Scope

This test is to determine if the PICC Type B respects the FSD size according to ISO/IEC 14443-4:2001, 7.10.4.

G.4.7.2 Procedure

Perform the following steps for each FSDI = 0 to 8:

a) Put the PICC into READY DECLARED SUB- state as described in G.4.4.1.1.

b) Send the ATTRIB(0, fsdi) command with parameter fsdi as in the particular test.

c) Check if the PICC answer is ATA(0).

d) Send the I-block $I(0)_0$(TEST_COMMAND2(2)).

e) Check if the size of the I-block response of the PICC response is ≤ FSD

G.4.7.3 Test report

Fill the appropriate row in "Table G.33 — Reported Results for Type B specific test methods" according to the test results as follows:

Explanation	Test result
Only when the PICC responded as indicated in the procedure	Pass
Any other case	Fail

G.5 Test methods for logical operation of the PICC of Type A/B

G.5.1 Introduction

This chapter contains tests verifying that the activated PICC conforms to the ISO/IEC 14443-4. This chapter applies to PICC of Type A and Type B.

G.5.1.1 PICC activation process

PICC activation is the process of putting the PICC in the state where protocol blocks defined in ISO/IEC 14443-4:2001 may be exchanged. This process is dependent on the PICC type.

G.5.1.1.1 Activation of the PICC Type A

a) Put the PICC into ACTIVE state as described in G.3.3.2.1.

b) Send RATS(cid, fsdi).

c) Check that the PICC response is a valid ATS.

G.5.1.1.2 Activation of the PICC Type B

a) Put the PICC into READY DECLARED sub-state as described in G.4.4.1.1.

b) Send ATTRIB(cid, fsdi).

c) Check that the PICC response is a valid ATA.

G.5.2 PICC reaction to ISO/IEC 14443-4 Scenarios

G.5.2.1 Scope

This test is to determine the reaction of the PICC in different protocol scenarios. These tests are concrete implementations of the protocol scenarios of ISO/IEC 14443-4:2001 Annex B.

G.5.2.2 Procedure

Perform the following steps for each of Scenario G.32 though Scenario G.52 listed in this subclause:

a) Activate the PICC as described in G.5.1.1, use CID=0 and FSDI=0.

b) For each Step in the Scenario do:

   1) Send the command as described in the PICC-test-apparatus column.

   2) Check that the PICC response matches the one of the PICC column.

c) End for.

Scenario G.32: Exchange of I-blocks

Step	PICC-test-apparatus		PICC
1	$I(0)_0$(TEST_COMMAND1(1))	⟶	
		⟵	$I(0)_0$(TEST_RESPONSE1(1))
2	$I(0)_1$(TEST_COMMAND1(1))	⟶	
		⟵	$I(0)_1$(TEST_RESPONSE1(1))

Scenario G.33: Request for waiting time extension

Step	PICC-test-apparatus		PICC
1	$I(0)_0$(TEST_COMMAND3)	⟶	
		⟵	S(WTX) (n)
2	S(WTX) (n)	⟶	
		⟵	$I(0)_0$(TEST_RESPONSE3)
3	$I(0)_1$(TEST_COMMAND1(1))	⟶	
		⟵	$I(0)_1$(TEST_RESPONSE1(1))

Scenario G.34: DESELECT

Step	PICC-test-apparatus		PICC
1	$I(0)_0$(TEST_COMMAND1(1))	⟶	
		⟵	$I(0)_0$(TEST_RESPONSE1(1))
2	S(DESELECT)	⟶	
		⟵	S(DESELECT)
3	REQA or REQB(1) [a]	⟶	
		⟵	Mute
4	WUPA or WUPB(1) [a]	⟶	
		⟵	ATQA or ATQB [a]

[a] For the PICC Type A, the left option shall be used. For the PICC Type B, the right option shall be used.

Scenario G.35: PCD uses chaining

Step	PICC-test-apparatus		PICC
1	$I(1)_0$ (TEST_COMMAND1(2)$_1$)	⟶	
		⟵	$R(ACK)_0$
2	$I(0)_1$(TEST_COMMAND1(2)$_2$)	⟶	
		⟵	$I(0)_1$(TEST_RESPONSE1(2))
3	$I(0)_0$(TEST_COMMAND1(1))	⟶	
		⟵	$I(0)_0$(TEST_RESPONSE1(1))

Scenario G.36: PICC uses chaining

Step	PICC-test-apparatus		PICC
1	$I(0)_0$(TEST_COMMAND2(2))	⟶	
		⟵	$I(1)_0$ (TEST_RESPONSE2(2)$_1$)
2	$R(ACK)_1$	⟶	
		⟵	$I(0)_1$ (TEST_RESPONSE2(2)$_2$)
3	$I(0)_0$(TEST_COMMAND1(1))	⟶	
		⟵	$I(0)_0$(TEST_RESPONSE1(1))

Scenario G.37: Start of protocol

Step	PICC-test-apparatus		PICC
1	$I(0)_0$(TEST_COMMAND1(1), ~CRC)	⟶	
		⟵	Mute
2	$R(NAK)_0$	⟶	
		⟵	$R(ACK)_1$
3	$I(0)_0$(TEST_COMMAND1(1))	⟶	
		⟵	$I(0)_0$(TEST_RESPONSE1(1))
4	$I(0)_1$(TEST_COMMAND1(1))	⟶	
		⟵	$I(0)_1$(TEST_RESPONSE1(1))

Scenario G.38: Exchange of I-blocks

Step	PICC-test-apparatus		PICC
1	$I(0)_0$(TEST_COMMAND1(1))	⟶	
		⟵	$I(0)_0$ (TEST_RESPONSE1(1))
2	$I(0)_1$ (TEST_COMMAND1(1), ~CRC)	⟶	
		⟵	Mute
3	$R(NAK)_1$	⟶	
		⟵	$R(ACK)_0$
4	$I(0)_1$ (TEST_COMMAND1(1))	⟶	
		⟵	$I(0)_1$(TEST_RESPONSE1(1))
5	$I(0)_0$(TEST_COMMAND1(1))	⟶	
		⟵	$I(0)_0$(TEST_RESPONSE1(1))

Scenario G.39: Exchange of I-blocks 1

Step	PICC-test-apparatus		PICC
1	$I(0)_0$(TEST_COMMAND1(1))	⟶	
		⟵	$I(0)_0$ (TEST_RESPONSE1(1))
2	$R(NAK)_0$	⟶	
		⟵	$I(0)_0$ (TEST_RESPONSE1(1))
3	$I(0)_1$ (TEST_COMMAND1(1))	⟶	
		⟵	$I(0)_1$(TEST_RESPONSE1(1))

Scenario G.40: Exchange of I-blocks 2

Step	PICC-test-apparatus		PICC
1	$I(0)_0$(TEST_COMMAND1(1))	⟶	
		⟵	$I(0)_0$ (TEST_RESPONSE1(1))
2	$R(NAK, \sim CRC)_0$	⟶	
		⟵	Mute
3	$R(NAK)_0$	⟶	
		⟵	$I(0)_0$ (TEST_RESPONSE1(1))

Step	PICC-test-apparatus		PICC
4	$I(0)_1$ (TEST_COMMAND1(1))	⟶	
		⟵	$I(0)_1$(TEST_RESPONSE1(1))

Scenario G.41: Request for waiting time extension

Step	PICC-test-apparatus		PICC
1	$I(0)_0$(TEST_COMMAND3)	⟶	
		⟵	S(WTX)(n)
2	$R(NAK)_0$	⟶	
		⟵	S(WTX)(n)
3	S(WTX)(n)	⟶	
		⟵	$I(0)_0$ (TEST_RESPONSE3)
4	$I(0)_1$ (TEST_COMMAND1(1))	⟶	
		⟵	$I(0)_1$(TEST_RESPONSE1(1))

Scenario G.42: Request for waiting time extension

Step	PICC-test-apparatus		PICC
1	$I(0)_0$ (TEST_COMMAND3)	⟶	
		⟵	S(WTX)(n)
2	$R(NAK, \sim CRC)_0$	⟶	
		⟵	Mute
3	$R(NAK)_0$	⟶	
		⟵	S(WTX)(n)
4	S(WTX)(n)	⟶	
		⟵	$I(0)_0$ (TEST_RESPONSE3)
5	$I(0)_1$ (TEST_COMMAND1(1))	⟶	
		⟵	$I(0)_1$(TEST_RESPONSE1(1))

Scenario G.43: Request for waiting time extension

Step	PICC-test-apparatus		PICC
1	$I(0)_0$(TEST_COMMAND3)	⟶	
		⟵	S(WTX)(n)
2	S(WTX)(n, ~CRC)	⟶	
		⟵	Mute
3	$R(NAK)_0$	⟶	
		⟵	S(WTX)(n)
4	S(WTX)(n)	⟶	
		⟵	$I(0)_0$(TEST_RESPONSE3)
5	$I(0)_1$ (TEST_COMMAND1(1))	⟶	
		⟵	$I(0)_1$(TEST_RESPONSE1(1))

Scenario G.44: Request for waiting time extension

Step	PICC-test-apparatus		PICC
1	$I(0)_0$(TEST_COMMAND3)	⟶	
		⟵	S(WTX)(n)
2	S(WTX)(n)	⟶	
		⟵	$I(0)_0$(TEST_RESPONSE3)
3	$R(NAK)_0$	⟶	
		⟵	$I(0)_0$(TEST_RESPONSE3)
4	$I(0)_1$ (TEST_COMMAND1(1))	⟶	
		⟵	$I(0)_1$(TEST_RESPONSE1(1))

Scenario G.45: Request for waiting time extension

Step	PICC-test-apparatus		PICC
1	$I(0)_0$(TEST_COMMAND3)	⟶	
		⟵	S(WTX)(n)
2	S(WTX)(n)	⟶	
		⟵	$I(0)_0$ (TEST_RESPONSE3)
3	$R(NAK, \sim CRC)_0$	⟶	
		⟵	Mute
4	$R(NAK)_0$	⟶	
		⟵	$I(0)_0$ (TEST_RESPONSE3)
5	$I(0)_1$ (TEST_COMMAND1(1))	⟶	
		⟵	$I(0)_1$(TEST_RESPONSE1(1))

Scenario G.46: DESELECT

Step	PICC-test-apparatus		PICC
1	$I(0)_0$(TEST_COMMAND1(1))	⟶	
		⟵	$I(0)_0$(TEST_RESPONSE1(1))
2	S(DESELECT, ~CRC)	⟶	
		⟵	Mute
3	S(DESELECT)	⟶	
		⟵	S(DESELECT)
4	REQA or REQB(1) [a]	⟶	
		⟵	Mute
5	WUPA or WUPB(1) [a]	⟶	
		⟵	ATQA or ATQB [a]

[a] For the PICC Type A, the left option shall be used. For the PICC Type B, the right option shall be used.

Scenario G.47: PCD uses chaining

Step	PICC-test-apparatus		PICC
1	$I(1)_0$(TEST_COMMAND1$(3)_1$)	⟶	
		⟵	$R(ACK)_0$
2	$R(NAK)_0$	⟶	
		⟵	$R(ACK)_0$
3	$I(1)_1$(TEST_COMMAND1$(3)_2$)	⟶	
		⟵	$R(ACK)_1$
4	$I(0)_0$(TEST_COMMAND1$(3)_3$)	⟶	
		⟵	$I(0)_0$ (TEST_RESPONSE1(3))
5	$I(0)_1$(TEST_COMMAND1(1))	⟶	
		⟵	$I(0)_1$ (TEST_RESPONSE1(1))

Scenario G.48: PCD uses chaining

Step	PICC-test-apparatus		PICC
1	$I(1)_0$ (TEST_COMMAND1(3)$_1$)	⟶	
		⟵	$R(ACK)_0$
2	$I(1)_1$(TEST_COMMAND1(3)$_2$, ~CRC)	⟶	
		⟵	Mute
3	$R(NAK)_1$	⟶	
		⟵	$R(ACK)_0$
4	$I(1)_1$(TEST_COMMAND1(3)$_2$)	⟶	
		⟵	$R(ACK)_1$
5	$I(0)_0$(TEST_COMMAND1(3)$_3$)	⟶	
		⟵	$I(0)_0$ (TEST_RESPONSE1(3))
6	$I(0)_1$(TEST_COMMAND1(1))	⟶	
		⟵	$I(0)_1$ (TEST_RESPONSE1(1))

Scenario G.49: PCD uses chaining

Step	PICC-test-apparatus		PICC
1	$I(1)_0$ (TEST_COMMAND1(3)$_1$)	⟶	
		⟵	$R(ACK)_0$
2	$R(NAK, \sim CRC)_0$	⟶	
		⟵	Mute
3	$R(NAK)_0$	⟶	
		⟵	$R(ACK)_0$
4	$I(1)_1$ (TEST_COMMAND1(3)$_2$)	⟶	
		⟵	$R(ACK)_1$
5	$I(0)_0$ (TEST_COMMAND1(3)$_3$)	⟶	
		⟵	$I(0)_0$ (TEST_RESPONSE1(3))
6	$I(0)_1$(TEST_COMMAND1(1))	⟶	
		⟵	$I(0)_1$ (TEST_RESPONSE1(1))

Scenario G.50: PICC uses chaining

Step	PICC-test-apparatus		PICC
1	$I(0)_0$(TEST_COMMAND2(3))	⟶	
		⟵	$I(1)_0$(TEST_RESPONSE2(3)$_1$)
2	R(ACK, ~CRC)$_1$	⟶	
		⟵	Mute
3	R(ACK)$_1$	⟶	
		⟵	$I(1)_1$(TEST_RESPONSE2(3)$_2$)
4	R(ACK)$_0$	⟶	
		⟵	$I(0)_0$(TEST_RESPONSE2(3)$_3$)
5	$I(0)_1$(TEST_COMMAND1(1))	⟶	
		⟵	$I(0)_1$ (TEST_RESPONSE1(1))

Scenario G.51: PICC uses chaining

Step	PICC-test-apparatus		PICC
1	$I(0)_0$(TEST_COMMAND2(3))	⟶	
		⟵	$I(1)_0$(TEST_RESPONSE2(3)$_1$)
2	R(ACK)$_1$	⟶	
		⟵	$I(1)_1$(TEST_RESPONSE2(3)$_2$)
3	R(ACK)$_1$	⟶	
		⟵	$I(1)_1$(TEST_RESPONSE2(3)$_2$)
4	R(ACK)$_0$	⟶	
		⟵	$I(0)_0$(TEST_RESPONSE2(3)$_3$)
5	$I(0)_1$ (TEST_COMMAND1(1))	⟶	
		⟵	$I(0)_1$ (TEST_RESPONSE1(1))

Scenario G.52: PICC uses chaining

Step	PICC-test-apparatus		PICC
1	$I(0)_0$(TEST_COMMAND2(2))	⟶	
		⟵	$I(1)_0$(TEST_RESPONSE2(2))$_1$
2	$R(NAK)_0$	⟶	
		⟵	$I(1)_0$(TEST_RESPONSE2(2)$_1$)
3	$R(ACK)_1$	⟶	
		⟵	$I(0)_1$(TEST_RESPONSE2(2)$_2$)
4	$I(0)_0$ (TEST_COMMAND1(1))	⟶	
		⟵	$I(0)_0$ (TEST_RESPONSE1(1))

Scenario G.53: PICC Presence Check Method 1

NOTE This scenario replaces an old scenario that was removed.

Step	PICC-test-apparatus		PICC	Comment
1	$I(empty)_0$	⟶		
		⟵	$I()_0$	
2	$I(0)_1$(TEST_COMMAND1(1))	⟶		
		⟵	$I(0)_1$ (TEST_RESPONSE1(1))	
3	$I(empty)_0$	⟶		
		⟵	$I()_0$	

Scenario G.54: PICC Presence Check Method 2

NOTE This scenario replaces an old scenario that was removed.

Step	PICC-test-apparatus		PICC	Comment
1	$R(NAK)_0$	⟶		
		⟵	$R(ACK)_1$	
2	$R(NAK)_0$	⟶		
		⟵	$R(ACK)_1$	

3	$I(0)_0$(TEST_COMMAND1(1))	⟶		
		⟵	$I(0)_0$ (TEST_RESPONSE1(1))	
4	$R(NAK)_1$	⟶		
		⟵	$R(ACK)_0$	
5	$I(0)_1$(TEST_COMMAND1(1))	⟶		
		⟵	$I(0)_1$ (TEST_RESPONSE1(1))	

G.5.2.3 Test report

Fill the appropriate rows in "Table G.34 — Reported Results for test methods common for the PICC Type A/B" according to the test results as follows:

Explanation	Test result
Only when the PICC responded as indicated in the procedure	Pass
Any other case	Fail

G.5.3 Handling of PICC error detection

G.5.3.1 Scope

This test is to determine the error detection mechanism of the PICC as described in ISO/IEC 14443-4:2001, 7.5.5.

G.5.3.2 Procedure

Perform the following steps for each of Scenario G.55 through Scenario G.57 listed in this subclause:

a) Place the reference PICC into the field.

b) Activate the PICC as described in G.5.1.1, use CID=0 and FSDI=0.

c) For each Step in scenario do:

   1) Send the command as described in the PICC-test-apparatus column.

   2) Check if the PICC response is as described in the PICC column.

d) End for.

NOTE The comment column of the following tables refers to the rules of ISO/IEC 14443-4:2001 also as amended in ISO/IEC 14443-4/Amd.1:2006, 7.5.3 – 7.5.5.

Scenario G.55: Bad CRC on I-block

Step	PICC-test-apparatus	PICC	Comment

1	$I(0)_0$(TEST_COMMAND1(1), ~CRC)	⟶		7.5.5 a
		⟵	Mute	
2	$I(0)_0$(TEST_COMMAND1(1))	⟶		
		⟵	$I(0)_0$ (TEST_RESPONSE1(1))	

Scenario G.56: Bad CRC on chained I-block

Step	PICC-test-apparatus		PICC	Comment
1	$I(1)_0$(TEST_COMMAND1$(2)_1$)	⟶		
		⟵	$R(ACK)_0$	
2	$I(0)_1$(TEST_COMMAND1$(2)_2$, ~CRC)	⟶		7.5.5 a
		⟵	Mute	
3	$I(0)_1$(TEST_COMMAND1$(2)_2$)	⟶		
		⟵	$I(0)_1$ (TEST_RESPONSE1(2))	

Scenario G.57: Bad CRC on S(WTX)-Block

Step	PICC-test-apparatus		PICC	Comment
1	$I(0)_0$(TEST_COMMAND3)	⟶		
		⟵	S(WTX) (n)	
2	S(WTX)(n, ~CRC)	⟶		7.5.5 a
		⟵	Mute	
3	S(WTX)(n)	⟶		
		⟵	$I(0)_0$(TEST_RESPONSE3)	

G.5.3.3 Test report

Fill the appropriate rows in “Table G.34 — Reported Results for test methods common for the PICC Type A/B” according to the test results as follows:

Explanation	Test result

Only when the PICC responded as indicated in the procedure	Pass
Any other case	Fail

G.5.4 PICC reaction on CID

G.5.4.1 Scope

This test is to determine the reaction of the PICC to CID coding according to ISO/IEC 14443-4:2001, 7.1.1.2.

G.5.4.2 Procedure

Perform the following steps for each of Scenario G.58 through Scenario G.62 listed in this subclause. Use the proper CID test case table depending upon whether the PICC supports CID or not.

For each row in the CID test case tables e.g. in Table G.28 — CID test case table (for PICCs which support CID) or Table G.29 — CID test case table (for PICCs which do not support CID) do:

a) Activate the PICC with cidass as indicated in the column Assigned CID.

b) Perform a block exchange as described in the corresponding Scenario. Use the cidcmd as described in the Command CID column in the CID test case table.

c) Check if the PICC response matches with the response as in the PICC column in the Scenario. If two response options are indicated for the PICC, then the unique expected response will be determined from the expected PICC response column in the CID Test case table.

Table G.28 — CID test case table (for PICCs which support CID)

Test No.[a]	**Assigned CID (cid_{ass})**	**Command CID (cid_{cmd})**	**Expected PICC response**
1	1	1	Response 1 of the test scenario
2	0	0	Response 1 of the test scenario
3	0	NO CID	Response 1 of the test scenario
4	1	NO CID	Response 2 of the test scenario (Mute)
5	0	1	Response 2 of the test scenario (Mute)
6	1	0	Response 2 of the test scenario (Mute)
7	2	1	Response 2 of the test scenario (Mute)
[a] Each test number in the table shall be tested with each of the scenarios described.			

Table G.29 — CID test case table (for PICCs which do not support CID)

Test No.[a]	Assigned CID (cid_{ass})	Command CID (cid_{cmd})	Expected PICC response
1	0	0	Response 2 of the test scenario (Mute)
2	0	NO CID	Response 1 of the test scenario
3	0	1	Response 2 of the test scenario (Mute)
4 [b]	1	NO CID	Response 1 of the test scenario

a Each test number in the table shall be tested with each of the scenarios described.
b Applies to Type A PICC only

Scenario G.58: CID on I-block

Step	PICC-test-apparatus		PICC
1	$I(0)_0$(TEST_COMMAND1(1), CID = cid_{cmd})	⟶	
		⟵	Response 1: $I(0)_0$(TEST_RESPONSE1(1), CID=cid_{cmd}) Response 2: Mute [a]
a Response 1 or response 2 according to Table G.28 — CID test case table (for PICCs which support CID) or Table G.29 — CID test case table (for PICCs which do not support CID).			

Scenario G.59: CID on I-block with chaining

Step	PICC-test-apparatus		PICC
1	$I(1)_0$ (TEST_COMMAND1$(2)_1$,CID = cid_{cmd})	⟶	
		⟵	Response 1: R(ACK, CID=cid_{cmd})$_0$ Response 2: Mute [a]
a Response 1 or response 2 according to Table G.28 — CID test case table (for PICCs which support CID) or Table G.29 — CID test case table (for PICCs which do not support CID).			

Scenario G.60: CID on R-block

Step	PICC-test-apparatus		PICC
1	$I(0)_0$(TEST_COMMAND2(3), CID [a] =cid_{ass})	⟶	
		⟵	$I(1)_0$ (TEST_RESPONSE2$(3)_1$, CID=cid_{ass})
2	R(ACK, CID [a]=cid_{cmd}) $_1$	⟶	
		⟵	Response 1: $I(1)_1$ (TEST_RESPONSE2$(3)_2$, CID[a]=cid_{cmd}) Response 2: Mute [b]
a For PICC not supporting CID, use no CID. b Response 1 or response 2 according to Table G.28 — CID test case table (for PICCs which support CID) or Table G.29 — CID test case table (for PICCs which do not support CID).			

Scenario G.61: CID on S(WTX)-Block

Step	PICC-test-apparatus		PICC
1	$I(0)_0$(TEST_COMMAND3, CID[a]=cid_{ass})	⟶	
		⟵	S(WTX)(n, CID=cid_{ass})
2	S(WTX)(n, CID[a]=cid_{cmd})	⟶	
		⟵	Response 1: $I(0)_0$(TEST_RESPONSE3, CID[a]=cid_{cmd}) Response 2: Mute [b]

a For PICC not supporting CID, use no CID.

b Response 1 or response 2 according to Table G.28 — CID test case table (for PICCs which support CID) or Table G.29 — CID test case table (for PICCs which do not support CID).

Scenario G.62: CID on S(DESELECT)-Block

Step	PICC-test-apparatus		PICC
1	S(DESELECT, CID=cid_{cmd})	⟶	
		⟵	Response 1: S(DESELECT, CID=cid_{cmd}) Response 2: Mute [a]

a Response 1 or response 2 according to Table G.28 — CID test case table (for PICCs which support CID) or Table G.29 — CID test case table (for PICCs which do not support CID).

G.5.4.3 Test report

Fill the appropriate row in “Table G.34 — Reported Results for test methods common for the PICC Type A/B” according to the test results as follows:

Explanation	Test result
Only when the PICC responded as indicated in the procedure	Pass
Any other case	Fail

G.5.5 PICC reaction on NAD

G.5.5.1 Scope

This test is to determine the reaction of the PICC to NAD coding according to ISO/IEC 14443-4:2001,7.1.1.3.

G.5.5.2 Procedure

Perform the following steps for each of Scenario G.63 through Scenario G.65 listed in this subclause.

Activate the PICC as described in clause PICC activation process G.5.1.1, use CID=0 and FSDI=0,

For each Step in scenario do:

a) Send the command as described in the PICC-test-apparatus column.

b) Check that the PICC response matches the one of the PICC column.

Let n be an arbitrary value of a valid NAD with b4 and b8 set to 0.

Scenario G.63: NAD on I-block (for PICCs supporting NAD)

Step	PICC-test-apparatus		PICC
1	$I(0)_0$ (TEST_COMMAND1(1), NAD=n)	⟶	
		⟵	$I(0)_0$ (TEST_RESPONSE1(1), containing NAD)

Scenario G.64: NAD on chained I-block (for PICCs supporting NAD)

Step	PICC-test-apparatus		PICC
1	$I(0)_0$(TEST_COMMAND2(3), NAD=n)	⟶	
		⟵	$I(1)_0$ (TEST_RESPONSE2$(3)_1$, containing NAD)
2	$R(ACK)_1$	⟶	
		⟵	$I(1)_1$ (TEST_RESPONSE2$(3)_2$, not containing NAD)

Scenario G.65: NAD on I-block (for PICCs not supporting NAD)

Step	PICC-test-apparatus		PICC
1	$I(0)_0$ (TEST_COMMAND1(1), NAD=n)	⟶	
		⟵	Mute

G.5.5.3 Test report

Fill the appropriate rows in “Table G.34 — Reported Results for test methods common for the PICC Type A/B” according to the test results as follows:

Explanation	Test result
If the scenario is not applicable for the PICC	Not applicable (NA)
Only when the PICC’s response is as indicated in the procedure	Pass
Any other case	Fail

G.6 Reported results

Table G.30 — Type A specific timing table

No	Parameter	ISO Reference	Minimum value	Maximum value	Measured Value(s)
1	Frame delay time PCD to PICC (for REQA,WUPA, ANTICOLLISION, SELECT commands)	ISO/IEC 14443-3:2001 6.1.2	Last bit (1)b ->1236/*fc* Last bit (0)b -> 1172/*fc*	Last bit (1)b ->1236/*fc* Last bit (0)b -> 1172/*fc*	
2	RATS and Deactivation frame waiting time	ISO/IEC 14443-4:2001, 8.1	Last bit (1)b ->1236/*fc* Last bit (0)b -> 1172/*fc*	65536/*fc* (~4,8 ms)	
3	Frame delay time PCD to PICC (for frames other than previous rows)	ISO/IEC 14443-3:2001 6.1.2 and ISO/IEC 14443-4:2001, 8.1	Last bit (1)b ->1236/*fc* Last bit (0)b -> 1172/*fc*	(256/*fs*) x 2^{FWI} (~302,06 µs x 2^{FWI})	FWI = Max FDT =

NOTE All timing values are calculated for carrier frequency *fc* = 13,56 MHz and bit rate = *fc*/128 (~106 kbit/s)..

Table G.31 — Type B specific timing table

No	Parameter	ISO Reference	Std min	Std Max	Measured Value(s)
1	SOF low	ISO/IEC 14443-3:2001, 7.1.4	10 etu (~94,40 µs)	11 etu (~103,83 µs)	
2	SOF high	ISO/IEC 14443-3:2001, 7.1.4	2 etu (~18,88 µs)	3 etu (~28,32 µs)	
3	EOF low	ISO/IEC 14443-3:2001, 7.1.5	10 etu (~94,40 µs)	11 etu (~103,83 µs)	
4	Bit boundaries	ISO/IEC 14443-3:2001, 7.1.1	(n – 1/8) etu	(n + 1/8) etu	
5	EGT PICC to PCD	ISO/IEC 14443-3:2001, 7.1.2	0 µs	19 µs	
6	TR0 for ATQB	ISO/IEC 14443-3:2001, 7.1.6	64/*fs* (~75,52 µs)	256/*fs* (~302,06 µs)	
7	TR1 for ATQB	ISO/IEC 14443-3:2001, 7.1.6	80/*fs* (~94,40 µs)	200/*fs* (~235,99 µs)	
8	TR0 Not ATQB	ISO/IEC 14443-3:2001, 7.1.6 ISO/IEC 14443-3:2001, 7.10.3	Value as defined in ISO/IEC 14443-3:2001, Table 31	(256/*fs*) x 2^{FWI} (~302,06 µs x 2^{FWI})	FWI = Max TR0 =

No	Parameter	ISO Reference	Std min	Std Max	Measured Value(s)
9	TR1 Not ATQB	ISO/IEC 14443-3:2001, 7.1.6 ISO/IEC 14443-3:2001, 7.10.3	Value as defined in ISO/IEC 14443-3:2001, Table 32	200/*fs* (~235,99 µs)	
10	TR2	ISO/IEC 14443-3 Amendment 1		According to table Amd.1-4	
11	Delay from the end of EOF and Subcarrier off	ISO/IEC 14443-3:2001, 7.1.7	0	2 etu	
12	Deactivation frame waiting time	ISO/IEC 14443-4:2001, 8.1	64/*fs* + 80/*fs* (~169,92 µs)	65536/*fc* (~4,8 ms)	

NOTE All timing values are calculated for carrier frequency *fc* = 13,56 MHz and bit rate = *fc*/128 (~106 kbit/s).

Table G.32 — Reported Results for Type A specific test methods

Test method from ISO/IEC 10373-6		Scenario Numbers	Test result
Clause	**Parameter**	**ISO/IEC 10373-6**	**PASS or FAIL orNA**
G.3.2	Polling	Scenario G.1	
G.3.3	Testing of the PICC Type A state transitions	Scenario G.2	
		Scenario G.3	
		Scenario G.4	
		Scenario G.5	
		Scenario G.6	
		Scenario G.7	
		Scenario G.8	
		Scenario G.9	
		Scenario G.10	
		Scenario G.11	
		Scenario G.12	
G.3.4	Handling of Type A anticollision	Scenario G.13	
G.3.5	Handling of RATS	Scenario G.14	
		Scenario G.15	
G.3.6	Handling of PPS request	Scenario G.16	
		Scenario G.17	
		Scenario G.18	
		Scenario G.19	
G.3.7	Handling of FSD	Scenario G.20	

Table G.33 — Reported Results for Type B specific test methods

Test method from ISO/IEC 10373-6		Scenario Numbers	Test Results
Clause	**Parameter**	**ISO/IEC 10373-6**	**PASS or FAIL or NA**
G.4.2	Polling	Scenario G.21	
G.4.3	PICC Reception	Scenario G.22	
G.4.4	Testing of the PICC Type B State Transitions	Scenario G.23	
		Scenario G.24	
		Scenario G.25	
		Scenario G.26	
		Scenario G.27	
G.4.5	Handling of Type B anticollision	Scenario G.28	
G.4.6	Handling of ATTRIB	Scenario G.29	
		Scenario G.30	
G.4.7	Scenario G.31 Handling of Maximum Frame Size	Scenario G.31	

Table G.34 — Reported Results for test methods common for the PICC Type A/B

Test method from ISO/IEC 10373-6		Test Scenario	Test Results
Clause	**Parameter**	**ISO/IEC 10373-6**	**PASS or FAIL orNA**
G.5.2	PICC reaction to ISO/IEC 14443-4 Scenarios	Scenario G.32	
		Scenario G.33	
		Scenario G.34	
		Scenario G.35	
		Scenario G.36	
		Scenario G.37	
		Scenario G.38	
		Scenario G.39	
		Scenario G.40	
		Scenario G.41	
		Scenario G.42	
		Scenario G.43	
		Scenario G.44	
		Scenario G.45	
		Scenario G.46	
		Scenario G.47	
		Scenario G.48	
		Scenario G.49	
		Scenario G.50	

Test method from ISO/IEC 10373-6		Test Scenario	Test Results
Clause	**Parameter**	**ISO/IEC 10373-6**	**PASS or FAIL orNA**
		Scenario G.51	
		Scenario G.52	
G.5.3	Handling of PICC error detection	Scenario G.53	
		Scenario G.54	
		Scenario G.55	
		Scenario G.56	
		Scenario G.57	
G.5.4	PICC reaction on CID	Scenario G.58	
		Scenario G.59	
		Scenario G.60	
		Scenario G.61	
		Scenario G.62	
G.5.5	PICC reaction on NAD	Scenario G.63	
		Scenario G.64	
		Scenario G.65	
G.1.5	Generating the I/O character timing in reception mode		
G.1.5.1	RFU values		

Annex H
(normative)

Additional PCD test methods

H.1 PCD-test-apparatus and accessories

This clause defines the PCD-test-apparatus and test circuits for verifying the operation of the PCD according to ISO/IEC 14443-3:2001 and ISO/IEC 14443-4:2001.

H.1.1 Test method

The ISO/IEC 9646 abstract model is chosen and the local test method is used for the testing of the ISO/IEC 14443 protocol between the tested PCD and the LT.

H.1.2 PCD-test-apparatus structure

The PCD-test-apparatus consists of two parts:

— Upper Tester (can be personal computer with a host interface suitable for a tested PCD)

— Lower Tester (LT)

Tested PCD is treated as Implementation Under Test (IUT).

When a PCD is embedded in a product, it includes the UT. For this case some tests may not be applicable. Also, in case the standard does not have a specific requirement the test method will end up in a report of capabilities only.

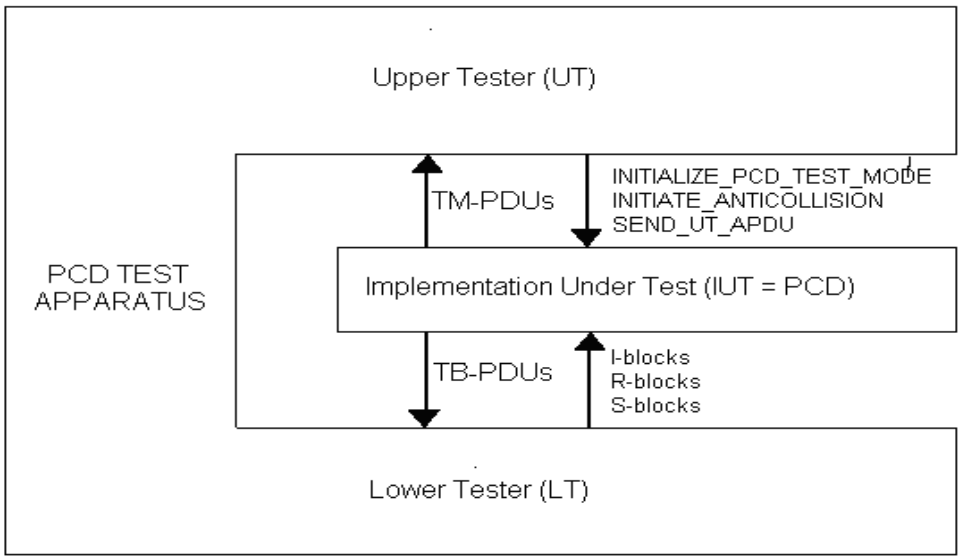


Figure H.1 — Conceptual tester architecture

The LT part of the PCD-test-apparatus includes:

— A PICC emulation hardware and software device capable of emulating of Type A and Type B protocols.

— Digital sampling oscilloscope (see ISO/IEC 10373-6:2001, 6.4)

H.1.3 PCD-test-apparatus interface

The UT and the IUT communicate with the TM-PDU (Test Management PDU). The definition of TM-PDUs is product dependent and provided by the IUT manufacturer.

	TM-PDU name	**Required IUT action**
1	INITIALIZE_PCD_TEST_MODE	Return to Power On state (The IUT is expected to enter to anticollision loop). The IUT returns the result code of its action to the UT.
2	INITIATE_ANTICOLLISION	Initiate anticollision sequence. (if the IUT starts the anticollision sequence automatically upon initialize, the sequence can be empty). The IUT returns the result code of its action to the UT.
3	SEND_UT_APDU	Transmit the UT_APDU through the RF interface to LT and return the IUT result code of its action to the UT. The response from the IUT shall include the answer of LT to the sent UT_APDU.

Figure H.2 — Logical interface commands

The PCD-test-apparatus shall be able to initialize the IUT utility information provided by the IUT manufacturer over the UT interface and to configure itself to perform the necessary procedures, protocols and analysis over its LT interface.

H.1.4 Emulating the I/O protocol

The PCD-test-apparatus at its LT interface shall be able to emulate the protocol Type A and Type B and PICC applications, which are required to run the Test Scenario. The LT shall be able to break the transmitted packets into chained blocks with the required length.

It shall be possible to configure the LT to simulate different options:

— NAD and CID configuration.

— Frame size, bit rates and any other parameter as required for the implementation of the test methods.

H.1.5 Generating the I/O character timing in transmission mode

The PCD-test-apparatus at its LT interface shall be able to generate the I/O bit stream according to ISO/IEC 14443-3:2001. Timing parameters: start bit duration, extra guard time (Type B only), bit duration, frame delay time, start of frame width and end of frame width shall be configurable. For the purpose of tests of Type A, the LT shall be capable of simulating a bit collision at a selected bit position(s).

H.1.6 Measuring and monitoring the RF I/O protocol

The PCD-test-apparatus at its LT interface shall be able to measure and monitor the timing of the logical low and high states transmitted by the PCD.

H.1.7 Protocol Analysis

The PCD-test-apparatus shall be able to analyze the I/O-bit stream at its LT interface in accordance with protocol Type A and Type B as specified in ISO/IEC 14443-3:2001 and ISO/IEC 14443-4:2001 and extract the logical data flow for further protocol analysis.

H.1.8 Protocol activation procedure

H.1.8.1 Activation procedure for anticollision test methods

Activate the LT by the following sequence:

c) Configure the LT to emulate the Type A or Type B protocol.

d) The UT sends INITIALIZE_PCD_TEST_MODE TM-PDU to the PCD.

e) The UT sends INITIATE_ANTICOLLISION TM-PDU to the PCD.

H.1.8.2 Activation procedure for Type A protocol test methods

Activate the LT by the following sequence:

a) Configure the LT to emulate the Type A protocol.

b) The UT sends INITIALIZE_PCD_TEST_MODE TM-PDU to the PCD.

c) The UT sends INITIATE_ANTICOLLISION TM-PDU to the PCD. The PCD shall apply the anticollision sequence as defined in ISO/IEC 14443-3:2001, Clause 6 (request, anticollision loop and select). The PCD shall apply the protocol activation sequence as defined in ISO/IEC 14443-4:2001, Clause 5.

d) The PCD reports the UT the result of the activation procedure.

H.1.8.3 Activation procedure for Type B protocol test methods

Activate the LT by the following sequence:

a) Configure the LT to emulate the Type B protocol.

b) The UT sends INITIALIZE_PCD_TEST_MODE TM-PDU to the PCD.

c) The UT sends INITIATE_ANTICOLLISION TM-PDU to the PCD. The PCD shall apply the anticollision sequence as defined in ISO/IEC 14443-3:2001, Clause 7.

d) The PCD reports the UT the result of the activation procedure.

H.1.9 Test scenario

H.1.9.1 Description

Testing of the PCD as defined in this document requires a Test Scenario to be executed. This Test Scenario is a 'typical protocol and application specific communication', dependent on the protocol and application specific functionality foreseen for the normal use of and implemented in the PCD.

The typical Test Scenario is the set of command TM-PDUs defined in H.1.3.

The Test Scenario shall be defined by the entity carrying out these tests and shall be documented with the test results. The Test Scenario shall encompass a representative subset or preferably, if practical, the full functionality of the PCD expected to be utilized during normal use.

NOTE The testing entity may require information about the implemented protocol and functionality.

The UT-APDU to be sent may be one from the following:

— UT_TEST_COMMAND1, decided by the PCD-test-apparatus, specifies the ISO instruction used as the default instruction for test scenarios not needing PCD chaining. (In case PCD decides anyway to chain, the test scenario should be adapted accordingly by the test laboratory).

— UT_TEST_COMMAND2, decided by the PCD-test-apparatus, specifies the ISO instruction used as the default instruction for test scenarios dealing with PCD chaining.

H.1.9.2 Test scenario example

The typical Test Scenario may be as follows:

```
INITIALIZE_PCD_TEST_MODE
INITIATE_ANTICOLLISION
SEND_UT_APDU (UT_TEST_COMMAND1)
SEND_UT_APDU (UT_TEST_COMMAND2)
….
```

H.1.10 UT, LT and PCD behaviour

The following items summarize the behaviour of the UT, the LT and the PCD:

a) The UT runs the activation procedure as defined in H.1.8.

b) If the activation procedure went wrong, the PCD goes to exception processing. This exception processing may include reporting the error to the UT.

c) In case of anticollision test methods the PCD-test-apparatus ends the test at this point. For protocol test methods the UT continues to the next step.

d) The UT sends the first command UT_APDU to the PCD.

e) The PCD is expected to transfer this command UT_APDU to the LT using TB-PDUs. The PCD splits the current UT-APDU into the appropriate TB-PDUs (I-blocks), sends the first I-block to LT and response block is awaited. The PCD manages communication blocks according to ISO/IEC 14443-4.

f) The command UT_APDU is received by the LT. The LT sends the response UT_APDU to the PCD. The LT manages communication blocks (TB-PDUs) according to ISO/IEC 14443-4 (the LT may use chaining mechanism at any time even if not mandated by either PCD or PICC maximum frame size). The PCD is expected to transfer response UT_APDU, received from the LT, back to the UT.

g) If the command failed at protocol level (i.e. error detected by the PCD), the PCD goes to exception processing. Exception processing may include error reporting to the UT.

h) If the command succeeded, the PCD reports the UT about successful result. In this case, if the test scenario defines additional UT-APDU to be sent to the LT, the UT sends the next UT-APDU to the PCD. This loop continues until the last test UT-APDU is sent.

H.1.11 Relationship of test methods versus base standard requirement

All tests shall be executed and reported in the corresponding tables.

Table H.1 — Type A specific test methods

Test method from ISO/IEC 10373-6		Corresponding requirement	
Clause	**Name**	**Base standard**	**Clauses**
H.2.1	Frame delay time PICC to PCD	ISO/IEC 14443-3:2001	6.1.3
H.2.2	Request Guard Time	ISO/IEC 14443-3:2001	6.1.4
H.2.3	Handling of bit collision during ATQA	ISO/IEC 14443-3:2001	6.4.2
H.2.4	Handling of anticollision loop	ISO/IEC 14443-3:2001	6.4.3
H.2.5	Handling of RATS and ATS	ISO/IEC 14443-4:2001	5.6.1.1
H.2.6	Handling of PPS response	ISO/IEC 14443-4:2001	5.6.2.1
H.2.7	Frame size selection mechanism	ISO/IEC 14443-4:2001	5.2
H.2.8	Handling of Start-up Frame Guard Time	ISO/IEC 14443-4:2001	5.2.5
H.2.9	Handling of the CID during activation by the PCD	ISO/IEC 14443-4:2001	5.6.3

Table H.2 — Type B specific test methods

Test method from ISO/IEC 10373-6		Corresponding requirement	
Clause	Name	Base standard	Clauses
H.3.1	I/O transmission timing	ISO/IEC 14443-3:2001	7.1
H.3.2	Frame size selection mechanism	ISO/IEC 14443-3:2001	7.9
H.3.3	Handling of the CID during activation by the PCD	ISO/IEC 14443-3:2001	7.10

Table H.3 — Test methods for logical operation

Test method from ISO/IEC 10373-6		Corresponding requirement	
Clause	Name	Base standard	Clauses
H.4.1	Handling of the polling loop	ISO/IEC 14443-3:2001	5
H.4.2	Reaction of the PCD to request for waiting time extension	ISO/IEC 14443-4:2001	7.3
H.4.3	Error detection and recovery	ISO/IEC 14443-4:2001	7.5.5
H.4.4	Handling of NAD during chaining	ISO/IEC 14443-4:2001	7.1.1.3

H.2 Type A specific test methods

H.2.1 Frame delay time PICC to PCD

The purpose of this test is to determine the timing between a PICC frame and the next PCD frame.

H.2.1.1 Apparatus

See H.1.

H.2.1.2 Procedure

Place the LT into the PCD operating volume.

During the following procedure the RF Input/Receive data shall be continuously monitored and verified correct to ISO/IEC 14443-2:2001. All signal transitions (level and timing) as well as the logical content of the communication shall be recorded.

Use the following sequence:

a) The UT performs the activation procedure according to H.1.8.1.

b) The LT waits until the PCD sends a valid REQA/WUPA Command frame.

c) The LT answers with a valid ATQA.

d) The LT waits until the PCD sends a valid Anticollision command according to Figure 6 in the ISO/IEC 14443-3:2001.

e) Measure the time between the last modulation transmitted by the LT and the first pause transmitted by the PCD (see ISO/IEC 14443-3:2001, 6.1.3).

H.2.1.3 Test report

Report the signal recording. Fill the item 1 of Table H.5 — Type A Specific Timing table with measured value of frame delay time and Table H.7 — Reported Results for Type A specific test methods.

H.2.2 Request Guard Time

The purpose of this test is to determine the Request Guard Time of two consecutive REQA/WUPA commands. This test is relevant for PCDs, which send consecutive REQA/WUPA.

H.2.2.1 Apparatus

See H.1.

H.2.2.2 Procedure

Place the LT into the PCD operating volume.

During the following procedure the RF Input/Receive data shall be continuously monitored and verified correct to ISO/IEC 14443-2:2001. All signal transitions (level and timing) as well as the logical content of the communication shall be recorded.

Use the following sequence:

a) The UT performs the activation procedure according to H.1.8.1.

b) The LT waits until the PCD sends a valid REQA/WUPA Command frame. The LT remains Mute.

c) The LT waits until the PCD sends a valid REQA/WUPA Command frame. The LT remains Mute.

d) Measure the time between the start bits of two consecutive REQA/WUPA (see ISO/IEC 14443-3:2001, 6.1.4).

H.2.2.3 Test report

Report the signal recording. Fill item 2 in Table H.5 — Type A Specific Timing table with measured value of request guard time and in the appropriate row in Table H.7 — Reported Results for Type A specific test methods.

H.2.3 Handling of bit collision during ATQA

The purpose of this test is to determine the handling of bit collision during ATQA by the PCD.

H.2.3.1 Apparatus

See H.1.

H.2.3.2 Procedure

Place the LT into the PCD operating volume.

Use the following sequence:

a) The UT performs the activation procedure according to H.1.8.1.

b) The LT waits until the PCD sends a valid REQA/WUPA Command frame.

c) Maintain the LT to answer with ATQA using simulation of the bit collision at bit N (N from 1 up to 16). Collision at a bit causes a collision also in associated parity bit.

d) Record the the content of the PCD response.

H.2.3.3 Expected result

The PCD shall start the bit oriented anticollision sequence.

H.2.3.4 Test report

Record the presence and the content of the PCD commands.

Fill the appropriate row in Table H.7 — Reported Results for Type A specific test methods according Figure H.3 — Result criteria for Handling of bit collision during ATQA:

Explanation	Test result
Only when the PCD starts the bit oriented anticollision loop	Pass
Any other case	Fail

Figure H.3 — Result criteria for Handling of bit collision during ATQA

H.2.4 Handling of anticollision loop

The purpose of this test is to determine the handling of bit anticollision loop according to ISO/IEC 14443-3:2001, 6.4.3.

H.2.4.1 Apparatus

See H.1.

H.2.4.2 Procedure

Place the LT into the PCD operating volume.

H.2.4.2.1 Procedure 1 (single size UID)

Use the following sequence:

a) The UT performs the activation procedure according to H.1.8.1.

b) The LT waits until the PCD sends a valid REQA/WUPA Command frame).

c) The LT answers with ATQA indicating bit frame anticollision and UID size: single (bits b8 and b7 equal (00)b).

d) The PCD shall send ANTICOLLISION Command '93 20' (cascade level 1).

e) The LT answers with UID CL1 ('uid0 uid1 uid2 uid3 BCC').

f) The PCD shall send SELECT Command '93 70 uid0 uid1 uid2 uid3 BCC CRC_A'.

g) The LT answers with SAK (cascade bit is cleared, b3 =0), indicating that UID is complete.

Scenario H.1 — Handling of anticollision loop for PICC with single size UID (Procedure 1)

Test	PCD		LT	Stage
REQA/WUPA	REQA/WUPA	→		
		←	ATQA (single size UID)	1
ANTICOLLISION Level 1	ANTICOLLISION Command Level 1 ('93 20')	→		
		←	UID CL1 ('uid0 uid1 uid2 uid3 BCC')	2
SELECT	SELECT Command ('93 70 uid0 uid1 uid2 uid3 BCC CRC_A')	→		
		←	SAK(complete)	3

H.2.4.2.1.1 Expected result

The PCD shall operate as described in Scenario H.1.

H.2.4.2.1.2 Test report

Record the presence, the content of the PCD commands.

Fill the appropriate row in **Fehler! Verweisquelle konnte nicht gefunden werden.** according to Figure H.4 — Results criteria for Handling of anticollision loop Handling of anticollision loop:

Explanation	Test result
Only when the PCD command sequence is as expected	Pass
Any other case	Fail

Figure H.4 — Results criteria for Handling of anticollision loop Handling of anticollision loop

H.2.4.2.2 Procedure 2 (double size UID)

Use the following sequence:

a) The UT performs the activation procedure according to H.1.8.1.

b) The LT waits until the PCD sends a valid REQA/WUPA Command frame).

c) The LT answers with ATQA indicating bit frame anticollision and UID size: double (bits b8 and b7 equal (01)b).

d) The PCD shall send ANTICOLLISION Command '93 20' (cascade level 1).

e) The LT answers with UID CL1 ('88 uid0 uid1 uid2 BCC').

f) The PCD shall send SELECT Command '93 70 88 uid0 uid1 uid2 BCC CRC_A'.

g) The LT answers with SAK (cascade bit is set, b3 = 1).

h) The PCD shall increase the cascade level and shall send ANTICOLLISION Command '95 20' (cascade level 2).

i) The LT answers with UID CL2 ('uid3 uid4 uid5 uid6 BCC').

j) The PCD shall send SELECT Command '95 70 uid3 uid4 uid5 uid6 BCC CRC_A'.

k) The LT answers with SAK (cascade bit is cleared, b3 = 0), indicating that UID is complete.

Scenario H.2 — Handling of anticollision loop for PICC with double size UID (Procedure 2)

Test	PCD		LT	Stage
REQA/WUPA	REQA/WUPA	→		
		←	ATQA (double size UID)	1
ANTICOLLISION Level 1	ANTICOLLISION Command Level 1 ('93 20')	→		
		←	UID CL1 ('88 uid0 uid1 uid2 BCC')	2
SELECT	SELECT Command ('93 70 88 uid0 uid1 uid2 BCC CRC_A')	→		
		←	SAK(cascade)	3
ANTICOLLISION Level 2	ANTICOLLISION Command Level 2 ('95 20')	→		
		←	UID CL2 ('uid3 uid4 uid5 uid6 BCC')	4
SELECT	SELECT Command ('95 70 uid3 uid4 uid5 uid6 BCC CRC_A')	→		
		←	SAK(complete)	5

H.2.4.2.2.1 Expected result

The PCD shall operate as described in Scenario H.2.

H.2.4.2.2.2 Test report

Record the presence, the content of the PCD commands.

Fill the appropriate row in Table H.7 — Reported Results for Type A specific test methods according to Figure H.5 — Result criteria for Handling of anticollision loop Procedure 2 (double size UID):

Explanation	Test result
Only when the PCD command sequence is as expected	Pass
Any other case	Fail

Figure H.5 — Result criteria for Handling of anticollision loop Procedure 2 (double size UID)

H.2.4.2.3 Procedure 3 (triple size UID)

Use the following sequence:

a) The UT performs the activation procedure according to H.1.8.1.

b) The LT waits until the PCD sends a valid REQA/WUPA Command frame).

c) The LT answers with ATQA indicating bit frame anticollision and UID size: triple (bits b8 and b7 equal (10)b).

d) The PCD shall send ANTICOLLISION Command '93 20' (cascade level 1).

e) The LT answers with UID CL1 ('88 uid0 uid1 uid2 BCC').

f) The PCD shall send SELECT Command '93 70 88 uid0 uid1 uid2 BCC CRC_A'.

g) The LT answers with SAK (cascade bit is set, b3 = 1).

h) The PCD shall increase the cascade level and shall send ANTICOLLISION Command '95 20' (cascade level 2).

i) The LT answers with UID CL2 ('88 uid3 uid4 uid5 BCC').

j) The PCD shall send SELECT Command '95 70 88 uid3 uid 4 uid5 BCC CRC_A'.

k) The LT answers with SAK (cascade bit is set, b3 = 1).

l) The PCD shall increase the cascade level and shall send ANTICOLLISION Command '97 20' (cascade level 3).

m) The LT answers with UID CL3 ('uid6 uid7 uid8 uid9 BCC').

n) The PCD shall send SELECT Command '97 70 uid6 uid7 uid8 uid9 BCC CRC_A'.

o) The LT answers with SAK (cascade bit is cleared, b3 = 0), indicating that UID is complete.

Scenario H.3 — Handling of anticollision loop for PICC with triple size UID (Procedure 3)

Test	PCD		LT	Stage
REQA/WUPA	REQA/WUPA	→		
		←	ATQA (triple size UID)	1
ANTICOLLISION Level 1	ANTICOLLISION Command Level 1 ('93 20')	→		
		←	UID CL1 ('88 uid0 uid1 uid2 BCC')	2
SELECT	SELECT Command ('93 70 88 uid0 uid1 uid2 BCC CRC_A')	→		
		←	SAK(cascade)	3
ANTICOLLISION Level 2	ANTICOLLISION Command Level 2 ('95 20')	→		
		←	UID CL2 ('88 uid3 uid4 uid5 BCC')	4
SELECT	SELECT Command ('95 70 88 uid3 uid4 uid5 BCC CRC_A')	→		
		←	SAK(cascade)	5
ANTICOLLISION Level 3	ANTICOLLISION Command Level 3 ('97 20')	→		
		←	UID CL3 ('uid6 uid7 uid8 uid9 BCC')	6
SELECT	SELECT Command ('97 70 uid6 uid7 uid8 uid9 BCC CRC_A')	→		
		←	SAK(complete)	7

H.2.4.2.3.1 Expected result

The PCD shall operate as described in

.

H.2.4.2.3.2 Test report

Record the presence, the content of the PCD commands.

Fill the appropriate row in Table H.7 — Reported Results for Type A specific test methods according to Figure H.6 — Result criteria for Handling of anticollision loop Procedure 3 (triple size UID):

Explanation	Test result
Only when the PCD command sequence is as expected	Pass
Any other case	Fail

Figure H.6 — Result criteria for Handling of anticollision loop Procedure 3 (triple size UID)

H.2.4.2.4 Procedure 4 (Full Bitwise Anticollision, single size UID)

Use the following sequence:

a) The UT performs the activation procedure according to H.1.8.1.

b) The LT waits until the PCD sends a valid REQA or WUPA Command frame.

c) The LT answers with ATQA indicating bit frame anticollision and UID size: single (bits b8 and b7 equal (00)b).

d) The PCD shall send ANTICOLLISION Command: '93 20'.

e) The LT answers by a stream of 40 bits by emulating a collision on every bit, including parity bits.

f) Repeat the steps g) to h) for values k from 1 to 31.

g) The PCD shall send ANTICOLLISION Command: '93' NVB $UIDTX_1[[1..k]]$, where $UIDTX_1[[1..k-1]]$ is either empty (i.e. k=1) or the value already known by the PCD and $UIDTX_1[[k]]$ is an arbitrary bit selected by the PCD.

h) The LT answers by a stream of 40 minus k bits by emulating a collision on every bit, including parity bits.

i) The PCD may optionally send ANTICOLLISION Command: '93 60' $UIDTX_1[[1..32]]$. In this case the LT answers with BCC.

NOTE This optional ANTICOLLISON command does not change the Stage number.

j) The PCD shall send SELECT Command '93 70' $UIDTX_1[[1..32]]$ BCC CRC_A, with BCC calculated by the PCD if it has not run the optional step i).

k) The LT answers with SAK (cascade bit is cleared, b3 = 0), indicating that UID is complete.

Scenario H.4 — Handling of full bitwise anticollision loop for PICC (Procedure 4)

Test	PCD		LT	Stage
REQA/WUPA	REQA/WUPA	→		1
		←	ATQA (single size UID)	
ANTICOLLISION	ANTICOLLISION Command ('93 20')	→		2
		←	40 bits full collision frame	
ANTICOLLISION (k bits UIDPARTIAL) $1 \le k \le 31$	ANTICOLLISION Command ('93' NVB $UIDTX_1$[[1..k]])	→		k+2
		←	40 minus k bits collision frame	
OPTIONAL ANTICOLLISION (32 bits UIDPARTIAL)	ANTICOLLISION Command ('93 60' $UIDTX_1$[[1..32]])	→		
		←	(BCC)	
SELECT	SELECT Command ('93 70' $UIDTX_1$[[1..32]] BCC CRC_A)	→		34
		←	SAK(complete)	

H.2.4.2.4.1 Expected result

The PCD shall operate as described in Scenario H.4.

H.2.4.2.4.2 Test report

Record the presence, the content of the PCD commands.

Fill the appropriate row in Table H.7 — Reported Results for Type A specific test methods according to Figure H.7 — Result criteria for Procedure 4 (Full Bitwise Anticollision, single size UID):

Explanation	Test result
Only when the PCD command sequence is as expected	Pass
Any other case	Fail

Figure H.7 — Result criteria for Procedure 4 (Full Bitwise Anticollision, single size UID)

H.2.5 Handling of RATS and ATS

The purpose of this test is to determine the handling of RATS and ATS by the PCD according to ISO/IEC 14443-4:2001, 5.6.1.1.

H.2.5.1 Apparatus

See H.1.

H.2.5.2 Procedure

Place the LT into the PCD operating volume.

H.2.5.2.1 Procedure 1

Use the following sequence:

a) The UT performs the activation procedure according to H.1.8.1.

b) The LT answers relevant anticollision messages and waits until the PCD sends a valid RATS command frame.

c) The LT does not respond to RATS (Mute).

d) The PCD may send a valid RATS command frame.

e) If the PCD has sent a second RATS, the LT does not respond to the RATS (Mute).

f) The PCD shall start the deactivation sequence defined in ISO/IEC 14443-4:2001, Clause 8.

g) Repeat the procedure with an erroneous ATS frame (use a bad CRC_A) instead of Mute.

Scenario H.6 — Handling of RATS and ATS, Procedure 1

Test	PCD		LT
Mute	RATS command frame (e.g.'E0 01 CRC_A')	→	
		←	Mute
	RATS command frame (e.g.'E0 01 CRC_A')	→	
		←	Mute
start deactivation	DESELECT	→	
erroneous ATS frame	RATS command frame (e.g.'E0 01 CRC_A')	→	
		←	erroneous ATS frame [a]
	RATS command frame (e.g.'E0 01 CRC_A')	→	
		←	erroneous ATS frame [a]
start deactivation	DESELECT	→	

[a] Determined in step g).

H.2.5.2.1.1 Expected result

The PCD shall operate in accordance with Scenario H.6.

H.2.5.2.1.2 Test report

Record the presence, the content of the PCD commands.

Fill the appropriate row in Table H.7 — Reported Results for Type A specific test methods according to Figure H.9 — Result criteria Procedure 1:

Explanation	Test result
Only when the PCD command sequence is as expected, including f)	Pass
Any other case	Fail

Figure H.9 — Result criteria Procedure 1

H.2.5.2.2 Procedure 2

Use the following sequence:

a) The UT performs the activation procedure according to H.1.8.1.

b) The LT answers relevant anticollision messages and waits until the PCD sends a valid RATS command frame.

c) The LT answers with a valid ATS without TA byte.

d) The PCD shall return the result code, in accordance with Figure H.2 — Logical interface commands, of its action to the UT.

e) The UT sends the SEND_UT_APDU(UT_TEST_COMMAND1) to the PCD.

f) The PCD is expected to send any I-block (including empty) to the LT, possibly after PICC presence check sequences.

Scenario H.7 — Handling of RATS and ATS, Procedure 2

Test	PCD		LT
correct ATS	RATS command frame (e.g.'E0 01 CRC_A')	→	
		←	ATS
continue operation	Any I-block (including empty)	→	

H.2.5.2.2.1 Expected result

The PCD command is expected according to the Scenario H.7.

H.2.5.2.2.2 Test report

Record the presence, the content of the PCD commands.

Fill the appropriate row in Table H.7 — Reported Results for Type A specific test methods according to Figure H.10 — Result criteria Procedure 2:

Explanation	Test result
Only when the PCD command sequence is as expected	Pass
Any other case	Fail

Figure H.10 — Result criteria Procedure 2

H.2.5.2.3 Procedure 3

In case the PCD does not use the optional retransmission of RATS according to ISO/IEC 14443-4:2001, 5.6.1.1, skip this procedure.

In case the PCD uses the optional retransmission of RATS according to ISO/IEC 14443-4:2001, 5.6.1.1 use the following sequence:

a) The UT performs the activation procedure according to H.1.8.1.

b) The LT answers relevant anticollision messages and waits until the PCD sends a valid RATS command frame.

c) When the PCD has transmitted the RATS, the LT does not respond to the RATS (Mute).

d) When the PCD has retransmitted the RATS, the LT answers with a valid ATS.

e) The PCD is expected to send any I-block (including empty) to the LT, possibly after PICC presence check sequences, or a PPS request.

f) Repeat the procedure with an erroneous ATS frame (use a bad CRC_A) instead of Mute.

Scenario H.8 — Handling of RATS and ATS, Procedure 3

Test	PCD		LT
erroneous ATS	RATS command frame (e.g.'E0 01 CRC_A')	→	
		←	Mute / erroneous ATS frame [a]
PCD retransmits RATS	RATS command frame (e.g.'E0 01 CRC_A')	→	
		←	ATS
Continue operation	Any I-block (including empty) or PPS request	→	

[a] Determined in step f).

H.2.5.2.3.1 Expected result

The PCD command is expected according to the Scenario H.8.

H.2.5.2.3.2 Test report

Record the presence, the content of the PCD commands.

Fill the appropriate row in Table H.7 — Reported Results for Type A specific test methods according to Figure H.12 — Result criteria Procedure 3:

Explanation	Test result
Only when the PCD command sequence is as expected	Pass
Any other case	Fail

Figure H.12 — Result criteria Procedure 3

H.2.6 Handling of PPS response

The purpose of this test is to determine the handling of the PPS request according to ISO/IEC 14443-4:2001, 5.6.2.1. This test is applicable only for the PCD, which uses Protocol and Parameter Selection mechanism as a part of the PICC activation sequence. In case the PCD does not use the PPS mechanism the test report column shall be empty.

H.2.6.1 Apparatus

See H.1.

H.2.6.2 Preliminary Procedure

Use the following sequence to put the PCD into the state required by this test:

a) Place the LT into the PCD operating volume.

b) The UT performs the activation procedure according to H.1.8.1.

c) The LT answers relevant anticollision messages and waits until the PCD sends the RATS.

d) The LT answers with ATS (with valid TA<>'00' indicating, that higher bit rates are supported and therefore PPS is supported by this PICC and thus the PCD may perform the PPS sequence).

H.2.6.2.1 Procedure 1

Use the following sequence immediately after procedure H.2.6.2:

a) The LT waits until the PCD sends a valid PPS Request. Ensure, that PPSS start byte, Parameter 0 and Parameter 1 do not include RFU values.

NOTE It is not mandatory to send a PPS request.

b) The LT answers with PPS response.

c) The UT sends the SEND_UT_APDU(UT_TEST_COMMAND1) to the PCD.

d) The PCD shall transmit I-block using the selected parameters, possibly after PICC presence check sequences.

Scenario H.9 — Handling of PPS request and response, Procedure 1

Test	PCD		LT
correct PPS response	PPS request	→	
		←	PPS response
Set parameters and continue operation	The I-block provided by the UT	→	

H.2.6.2.1.1 Expected result

The PCD command is expected according to the Scenario H.9. Ensure, that PPSS start byte, Parameter 0 and Parameter 1 do not include RFU values.

H.2.6.2.1.2 Test report

Record the presence, the content of the PCD commands.

Fill the appropriate row in Table H.7 — Reported Results for Type A specific test methods according to Figure H.13 — Result criteria for Handling of PPS response Procedure 1:

Explanation	Test result
Only when the PCD command sequence is as expected and PPS request command does not include RFU values	Pass
Any other case	Fail

Figure H.13 — Result criteria for Handling of PPS response Procedure 1

H.2.6.2.2 Procedure 2

Use the following sequence immediately after procedure H.2.6.2:

a) The LT waits until the PCD sends a valid PPS Request.

b) The LT answers with erroneous PPS response (use a bad CRC_A).

c) The PCD may retransmit a valid PPS Request or continue operation (e.g. send an I-block), both using the default bit rate.

d) Repeat the procedure with no response to the PPS Request (Mute).

Scenario H.10 — Handling of PPS request and response, Procedure 2

Test	PCD		LT
erroneous PPS response or Mute	PPS request	→	
		←	Erroneous PPS response or Mute [a]
	Optional PPS request or an I-block	→	

[a] Determined in step d)

H.2.6.2.2.1 Expected result

The PCD command is expected according to the Scenario H.10.

H.2.6.2.2.2 Test report

Record the presence, the content of the PCD commands.

Fill the appropriate row in Table H.7 — Reported Results for Type A specific test methods according to Figure H.14 — Result criteria for Handling of PPS response Procedure 2:

Explanation	Test result
Only when the PCD command sequence is as expected	Pass
Any other case	Fail

Figure H.14 — Result criteria for Handling of PPS response Procedure 2

H.2.7 Frame size selection mechanism

The purpose of this test is to verify the correct handling of transmitted frame size. The transmitted frames shall not be longer than FSCI indication. This test shall be executed for at least FSCI set to 0, 1 and 8.

H.2.7.1 Apparatus

See H.1.

H.2.7.2 Procedure

Place the LT into the PCD operating volume.

Use the following sequence:

a) The UT performs the activation procedure according to H.1.8.1.

b) The LT answers relevant anticollision messages and waits until the PCD sends a valid RATS command frame.

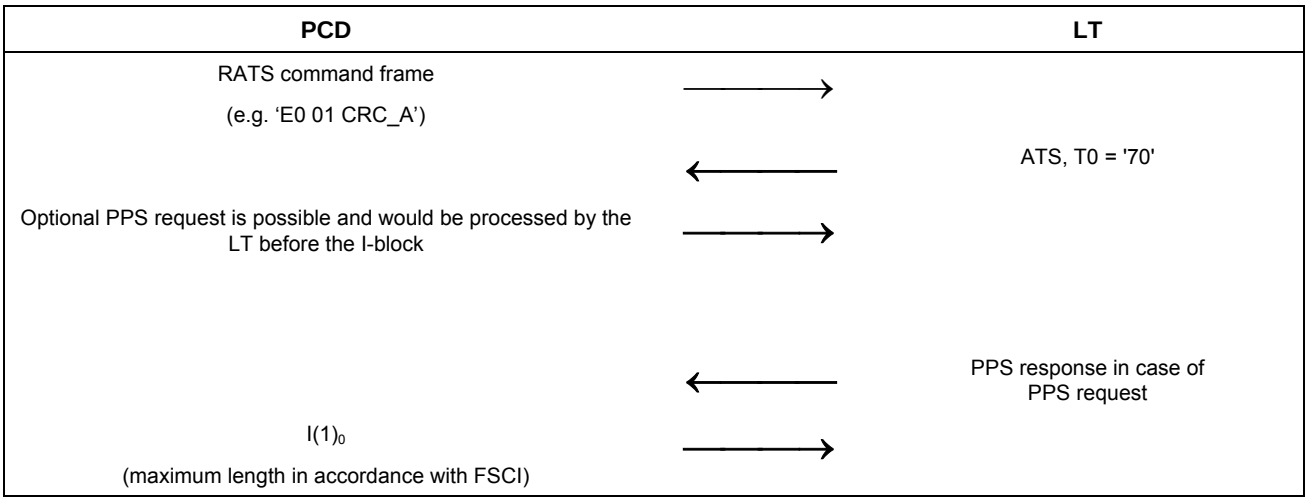
c) The LT answers with a valid ATS. For the purpose of this test, the LT returns format byte T0 equal '70' (see ISO/IEC 14443-4:2001, 5.2.3). In case there is a PPS request the LT will answer it before continuing with the next step:

   Maximum size of a frame accepted by the LT is in accordance with FSCI.

d) The UT sends the SEND_UT_APDU(UT_TEST_COMMAND2) to the PCD where the data length shall be more than the maximum size of a frame accepted by the LT.

e) The PCD shall send the following $I(1)_0$ block with maximum length of in accordance with FSCI.

Scenario H.11 — Frame size selection mechanism



H.2.7.3 Expected result

The PCD shall answer as described in Scenario H.11 for all tested FSCI values.

H.2.7.4 Test report

Fill the appropriate row in Table H.7 — Reported Results for Type A specific test methods according to Figure H.15 — Result criteria for Frame size selection mechanism:

Explanation	Test result
Only when the PCD's behaviour matches the expected Test Scenario exactly	Pass
When the PCD fails on any step of the Test Scenario	Fail

Figure H.15 — Result criteria for Frame size selection mechanism

H.2.8 Handling of Start-up Frame Guard Time

The purpose of this test is to determine the PCD transmission timing according to ISO/IEC 14443-4:2001, 5.2.5.

This test shall be executed for at least SFGI set to 0, 1 and 14.

H.2.8.1 Apparatus

See H.1.

H.2.8.2 Procedure

Place the LT into the PCD operating volume.

During the following procedure the RF Input/Receive data shall be continuously monitored and verified correct to ISO/IEC 14443-2:2001. All signal transitions (level and timing) as well as the logical content of the communication shall be recorded.

Use the following sequence:

a) The UT performs the activation procedure according to H.1.8.1.

b) The LT answers relevant anticollision messages and waits until the PCD sends a valid RATS command frame.

c) The LT answers with a valid ATS. For the purpose of this test the LT returns interface byte TB (1) equal '0E' (see ISO/IEC 14443-4:2001, 5.2.5). In case there is a PPS request the LT will answer it before continuing with the next step.

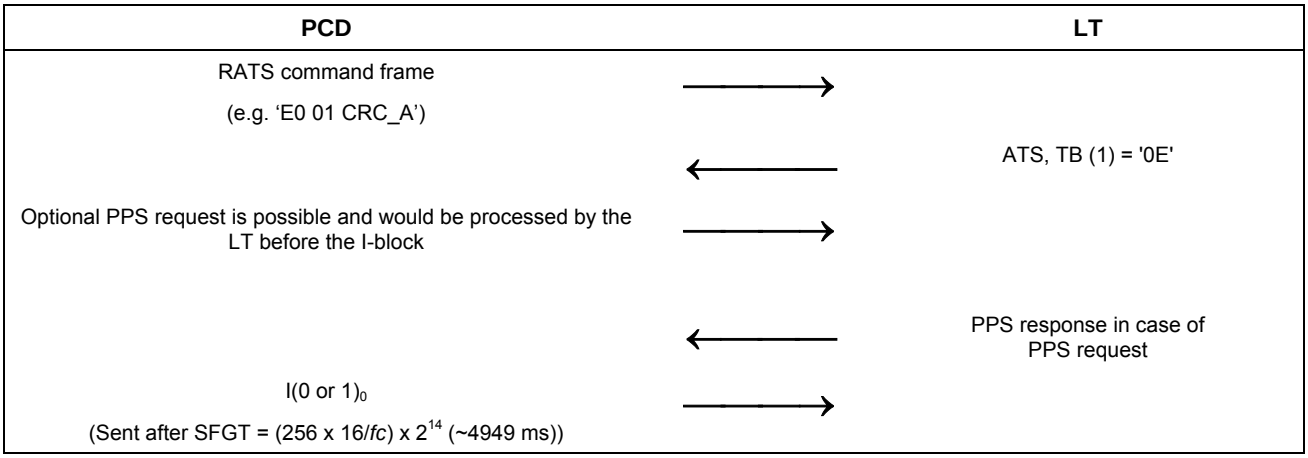
   Value '0E' = (00001110) b means:

   Minimum value of the frame delay accepted by the LT is (256 x 16/*fc*) x 2^{14} (~4949 ms).

d) The UT sends the SEND_UT_APDU(UT_TEST_COMMAND1) to the PCD.

e) The PCD shall send the following I(0 or 1)$_0$ block after a minimum delay of ~4949 ms.

Scenario H.12 — Start-up Frame Guard Time mechanism



H.2.8.3 Expected result

The PCD command is expected according to the Scenario H.12 for all tested FSGI values.

H.2.8.4 Test report

Fill the appropriate row in Table H.7 — Reported Results for Type A specific test methods according to Figure H.16 — Result criteria for Handling of Start-up Frame Guard Time:

Explanation	Test result
Only when the PCD's behaviour always matches the expected Test Scenario exactly	Pass
When the PCD fails on any step of the Test Scenario	Fail

Figure H.16 — Result criteria for Handling of Start-up Frame Guard Time

H.2.9 Handling of the CID during activation by the PCD

The purpose of this test is to determine the handling of the CID according to ISO/IEC 14443-4:2001, 5.6.3. This test shall be executed for at least CID set to 0, 1 and 14 if the CID can be chosen by the UT. Else, only the CID chosen by the PCD shall be used.

H.2.9.1 Apparatus

See H.1.

H.2.9.2 Procedure

Use the sequence a) to c) to put the PCD into the state required by this test:

a) Place the LT into the PCD operating volume.

b) The UT performs the activation procedure according to H.1.8.1.

c) The LT answers relevant anticollision messages and waits until the PCD sends the RATS. The LT answers with ATS.

For each test from the "Scenario H.13 — Handling of the CID", when supported by the PCD, use the sequence d) to h):

d) Put the PCD into the state required by this test.

e) The LT waits until the PCD applies the command as described in PCD column.

f) The LT answers as described in the LT column.

g) The UT sends the SEND_UT_APDU(UT_TEST_COMMAND1) to the PCD.

h) The PCD is expected to send I-block to the LT applying the condition as described in the PCD column.

Scenario H.13 — Handling of the CID

Test	PCD		LT
CID=n not equal to 0 and receive CID is supported	RATS (CID not equal 0)	→	
		←	ATS (CID supported)
	any valid command using CID	→	
CID=n not equal to 0 and receive CID is not supported	RATS (CID not equal 0)	→	
		←	ATS (CID not supported)
	any valid command without CID	→	
CID=n equal to 0 and receive CID is supported	RATS (CID equal to 0)	→	
		←	ATS (CID supported)
	any valid command using CID=0 or without CID	→	
CID=n equal to 0 and receive CID is not	RATS (CID equal to 0)	→	

Test	PCD	LT
supported	←	ATS (CID not supported)
	any valid command without CID →	

H.2.9.3 Expected result

The PCD's behaviour shall match the expected Test Scenario H.13 exactly.

H.2.9.4 Test report

Record the presence, the content of the PCD commands.

Fill the appropriate row in Table H.7 — Reported Results for Type A specific test methods according to Figure H.17 — Result criteria for Handling of the CID during activation by the PCD:

Explanation	Test result
Only when the PCD command sequence is as expected	Pass
Any other case	Fail

Figure H.17 — Result criteria for Handling of the CID during activation by the PCD

H.3 Type B specific test methods

H.3.1 I/O transmission timing

The purpose of this test is to determine the PCD transmission timing according to ISO/IEC 14443-3:2001, 7.1.

H.3.1.1 Apparatus

See H.1.

H.3.1.2 Procedure

Place the LT into the PCD operating volume.

During the following procedure the RF Input/Receive data shall be continuously monitored and verified correct to ISO/IEC 14443-2:2001. All signal transitions (level and timing) as well as the logical content of the communication shall be recorded.

a) The UT performs the activation procedure according to H.1.8.1.

b) Analyse the bit boundaries timing within a character sent by the PCD (see ISO/IEC 14443-3:2001, 7.1.1).

c) Analyse the extra guard time (EGT) between 2 consecutive characters sent by the PCD (see ISO/IEC 14443-3:2001, 7.1.2).

d) Analyse the timing of SOF sent by the PCD (see ISO/IEC 14443-3:2001, 7.1.4).

e) Analyse the timing of EOF sent by the PCD (see ISO/IEC 14443-3:2001, 7.1.5).

f) Analyse the timing before the PCD SOF (see ISO/IEC 14443-3:2001, 7.1.7).

H.3.1.3 Test report

Fill "**Fehler! Verweisquelle konnte nicht gefunden werden.**" with measured values from b) up to f) and appropriate row in **Fehler! Verweisquelle konnte nicht gefunden werden.**.

H.3.2 Frame size selection mechanism

The purpose of this test is to analyse the frame size selection mechanism according to ISO/IEC 14443-3:2001, 7.9.

This test shall be executed for at least Maximum Frame Size Code set to 0, 1 and 8.

H.3.2.1 Apparatus

See H.1.

H.3.2.2 Procedure

Place the LT into the PCD operating volume.

Use the following sequence:

a) The UT performs the activation procedure according to H.1.8.1.

b) The LT waits until the PCD sends a valid REQB/WUPB Command frame.

c) The LT answers with ATQB. Assume, that PUPI of the LT is '12 23 34 45' and the LT supports CID. For the purpose of this test the LT returns the second protocol info byte equal '01' (see ISO/IEC 14443-3:2001, 7.9.4), which means that maximum frame size supported by the LT is 16 bytes and the LT is compliant with ISO/IEC 14443-4.

d) The PCD shall send a valid ATTRIB Command frame.

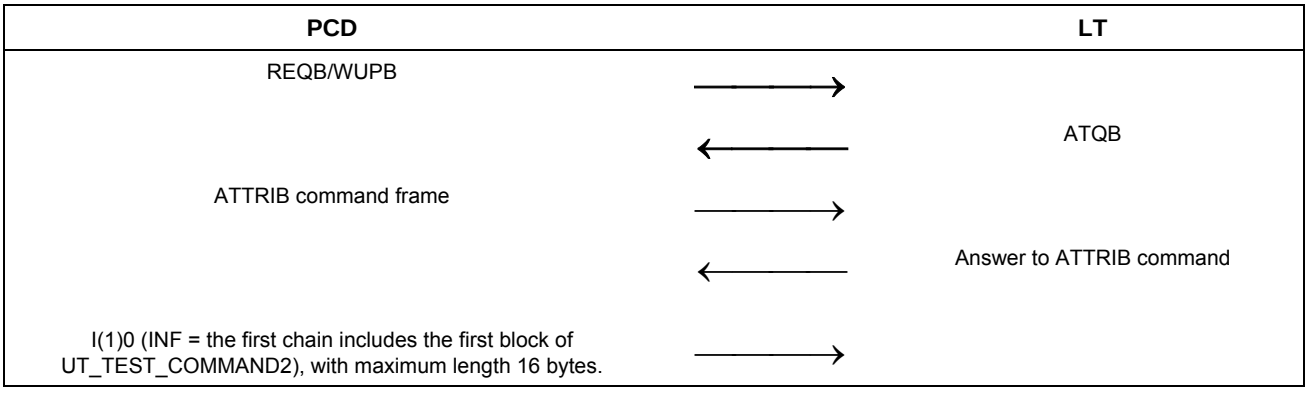
e) The LT sends Answer to ATTRIB command.

f) The PCD informs the UT of the end of the activation procedure.

g) The UT sends the SEND_UT_APDU(UT_TEST_COMMAND2) to the PCD.

h) The PCD shall send an $I(1)_0$ block with maximum length of 16 bytes as shown in the table PCD column.

Scenario H.14 — Frame size selection mechanism



H.3.2.3 Expected result

The PCD command is expected according to the Scenario H.14.

H.3.2.4 Test report

Fill the appropriate row in Table H.9 — Reported Results for Type B specific tests methods according to Figure H.18 — Result criteria for Frame size selection mechanism:

Explanation	Test result
Only when the PCD's behaviour always matches the expected Test Scenario exactly for at least Maximum Frame Size Code set to 0, 1 and 8	Pass
When the PCD fails on any step of the Test Scenario	Fail

Figure H.18 — Result criteria for Frame size selection mechanism

H.3.3 Handling of the CID during activation by the PCD

The purpose of this test is to determine the handling of the CID according to ISO/IEC 14443-3:2001.

This test shall be executed for at least CID set to 0, 1 and 14 if the CID can be chosen by the UT. Else, only the CID chosen by the PCD shall be used.

H.3.3.1 Apparatus

See H.1.

H.3.3.2 Procedure

Place the LT into the PCD operating volume.

H.3.3.2.1 Procedure 1

Use the following sequence:

a) The UT performs the activation procedure according to H.1.8.1.

b) The LT waits until the PCD sends the REQB/WUPB command.

c) The LT sends ATQB with Frame Option bits (b2,b1) equal (00)b. It means: CID and NAD are not supported.

d) The LT waits until the PCD sends the ATTRIB command. The PCD shall send a valid ATTRIB Command frame with PARAM4 byte equals 0.

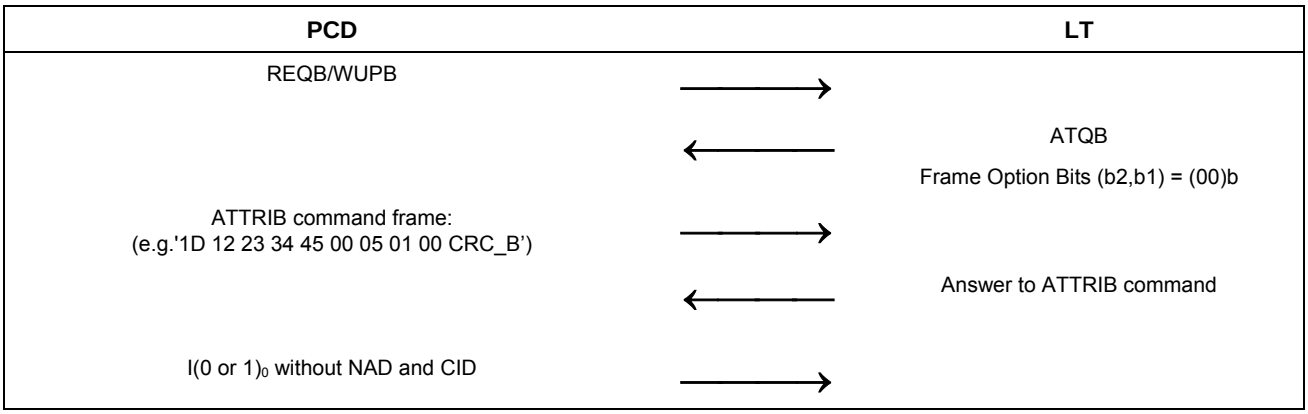
e) The LT sends Answer to ATTRIB command with CID value equals 0.

f) The PCD shall return the result code, in accordance with Figure H.2 — Logical interface commands, of its action to the UT.

g) The UT sends the SEND_UT_APDU(UT_TEST_COMMAND1) to the PCD.

h) The PCD shall send the following $I(0 \text{ or } 1)_0$ block without NAD and CID.

Scenario H.15 — Handling of the CID, Procedure 1



H.3.3.2.1.1 Expected result

The PCD's behaviour shall match the expected Test Scenario H.15 exactly.

H.3.3.2.1.2 Test report

Fill the appropriate row in Table H.9 — Reported Results for Type B specific tests methods according to Figure H.19 — Report criteria for Handling of the CID during activation by the PCD Procedure 1:

Explanation	Test result
Only when the PCD command sequence is as expected	Pass
Any other case	Fail

Figure H.19 — Report criteria for Handling of the CID during activation by the PCD Procedure 1

H.3.3.2.2 Procedure 2

Use the following sequence:

a) The UT performs the activation procedure according to H.1.8.1.

b) The LT waits until the PCD sends the REQB/WUPB command.

c) The LT sends ATQB with Frame Option bits (b2,b1) equal (01)b. It means: CID is supported and NAD is not supported.

d) The LT waits until the PCD sends the ATTRIB command. The PCD shall send a valid ATTRIB Command frame, using PARAM4 byte equals '0X' (CID = X in the range from 0 to 14).

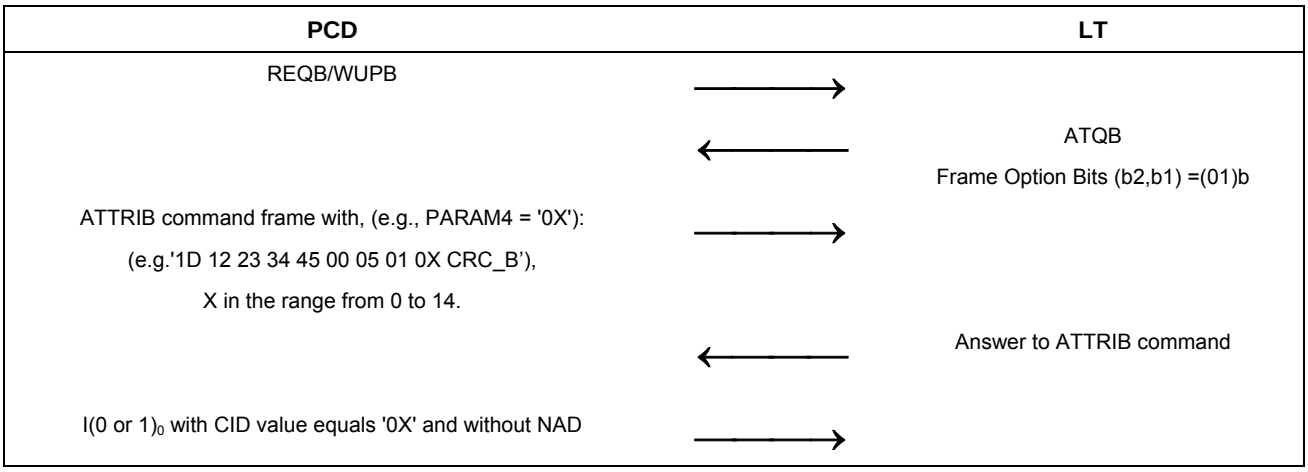
e) The LT sends Answer to ATTRIB command with CID value assigned by the PCD on step d) in PARAM4 byte.

f) The PCD shall return the result code, in accordance with Figure H.2 — Logical interface commands, of its action to the UT.

g) The UT sends the SEND_UT_APDU(UT_TEST_COMMAND1) to the PCD.

h) The PCD shall send the following I(0 or 1)$_0$ block using CID value assigned by the PCD on step d) or, optionally, using no CID if CID=0. The PCD shall not use NAD in this I(0 or 1)$_0$ block.

Scenario H.16 — Handling of the CID, Procedure 2



H.3.3.2.2.1 Expected result

The PCD's behaviour shall match the expected Test Scenario H.16 exactly.

H.3.3.2.2.2 Test report

Fill the appropriate row in Table H.9 — Reported Results for Type B specific tests methods according to Figure H.20 — Result criteria for Handling of the CID during activation by the PCD Procedure 2:

Explanation	Test result
Only when the PCD command sequence is as expected	Pass
Any other case	Fail

Figure H.20 — Result criteria for Handling of the CID during activation by the PCD Procedure 2

H.4 Test method for logical operations of the PCD

All test methods described in this clause, except H.4.1, shall be applied twice, once for Type A signal interface and once for Type B signal interface.

H.4.1 Handling of the polling loop

The purpose of this test is to determine the behaviour of the PCD during polling.

H.4.1.1 Apparatus

See H.1.

H.4.1.2 Procedure

Place the LT into the PCD operating volume.

During the following procedure the RF Input/Receive data shall be continuously monitored and verified correct to ISO/IEC 14443-2:2001. All signal transitions (level and timing) as well as the logical content of the communication shall be recorded.

Use the following sequence:

a) The UT performs the protocol activation procedure according to H.1.8.1.

b) The LT waits until the PCD sends a valid REQA/WUPA Command frame and a valid REQB/WUPB Command frame, in any order and repetition.

H.4.1.3 Expected result

The time between the end of REQA/WUPA (or the last REQA/WUPA of a series) and the beginning of REQB/WUPB (or the first REQB/WUPB of a series) shall be at least 5 ms.

The time between the end of REQB/WUPB (or the last REQB/WUPB of a series) and the beginning of REQA/WUPA (or the first REQA/WUPA of a series) shall be at least 5 ms.

H.4.1.4 Test report

Fill the appropriate row in Table H.11 — Reported Results for tests methods considering results for both for Type A and Type B according to Figure H.21 — Result criteria for Handling of the polling loop:

Explanation	Test result
Only when the PCD sends at least once REQA/WUPA and at least once REQB/WUPB command frames (at least 5 ms between each type).	Pass
In any other case	Fail

Figure H.21 — Result criteria for Handling of the polling loop

H.4.2 Reaction of the PCD to request for waiting time extension

The purpose of this test is to determine the behaviour of the PCD when the PICC uses a request for a waiting time extension (see ISO/IEC 14443-4:2001, 7.3). The mechanism of maintenance of WTX by the PCD is tested too.

This test shall be executed for at least FWI set to 0, 1 and 14 with TR0 and TR1 set to designate the default value in the LT, if it emulates a Type B PICC.

This test combination shall be executed for WTXM set at least to 1, 3 and 59 according to Table H.4 — Minimum combinations:

Table H.4 — Minimum combinations

Combination	FWI	WTXM
1	0	1
2	0	3
3	0	59
4	1	1
5	1	3
6	1	59
7	14	1
8	14	3
9	14	59

H.4.2.1 Apparatus

See H.1.

H.4.2.2 Procedure

Place the LT into the PCD operating volume.

During the following procedure the RF Input/Receive data shall be continuously monitored and verified correct to ISO/IEC 14443-2:2001. All signal transitions (level and timing) as well as the logical content of the communication shall be recorded.

The UT performs the protocol activation procedure according to H.1.8.2 for Type A or H.1.8.3 for Type B.

H.4.2.2.1 Procedure 1 (ISO/IEC 14443-4:2001, 7.3)

Use the following sequence immediately after procedure H.4.2.2:

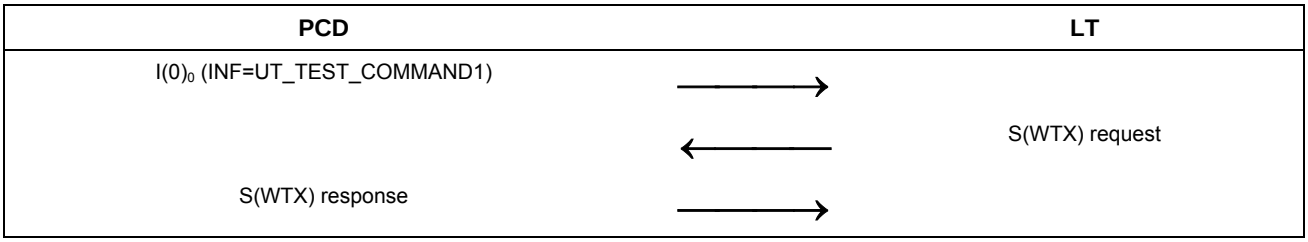
a) The UT sends the SEND_UT_APDU(UT_TEST_COMMAND1) to the PCD.

b) The LT waits until the PCD sends block $I(0)_0$ to the LT, with the INF field containing the UT_TEST_COMMAND1.

c) The LT sends S(WTX) request for a waiting time extension.

d) The PCD shall send S(WTX) response with INF(b6 to b1)=WTXM used.

Scenario H.17 —The PCD reaction to the LT waiting time extension request, procedure 1



H.4.2.2.1.1 Expected result

The PCD command is expected according to the Scenario H.17 for all FWI and WTXM values defined in H.4.2 in all combinations tested. The minimum combination is given in Table H.4 — Minimum combinations. The test shall only pass when every performed test passed.

H.4.2.2.1.2 Test report

Fill the appropriate row in Table H.11 — Reported Results for tests methods considering the test results both for Type A and Type B according to Figure H.22 — Result criteria for Reaction of the PCD to request for waiting time extension Procedure 1 (ISO/IEC 14443-4:2001, 7.3):

Explanation	Test result
Only when the PCD sends S(WTX) response with INF(b6 to b1) = WTXM	Pass
In any other case	Fail

Figure H.22 — Result criteria for Reaction of the PCD to request for waiting time extension Procedure 1 (ISO/IEC 14443-4:2001, 7.3)

H.4.2.2.2 Procedure 2 (ISO/IEC 14443-4:2001, 7.3)

Use the following sequence immediately after procedure H.4.2.2:

a) The UT sends the SEND_UT_APDU(UT_TEST_COMMAND1) to the PCD.

b) The LT waits until the PCD sends an I-block to the LT with the INF field containing the UT_TEST_COMMAND1.

c) The LT sends S(WTX) request.

d) The PCD shall send S(WTX) response with INF(b6 to b1)=WTXM. If it does not meet the expected response, end the test at this point.

e) Set the following bit-timing-parameters at the LT:

Parameter	Value	Reference
Temporary frame waiting time FWT_{TEMP}	WTXM x (256 x 16/fc) x 2^{FWI}	ISO/IEC 14443-3:2001, 7.9.4.3 ISO/IEC 14443-4:2001, 7.2 and 7.3
EGT as defined in ISO/IEC 14443-4	Maximum (19 µs)	ISO/IEC 14443-3:2001, 7.1.2
NOTE The Frame response time is defined as the time between the trailing edge of the EOF of the frame received and the leading edge of the SOF of the next frame sent.		

f) The LT sends the answer to the command UT_TEST_COMMAND1, sent in b).

g) The PCD is expected to transfer the response UT_APDU (answer to the command UT_TEST_COMMAND1) back to the UT.

h) The UT sends the SEND_UT_APDU(UT_TEST_COMMAND1) to the PCD.

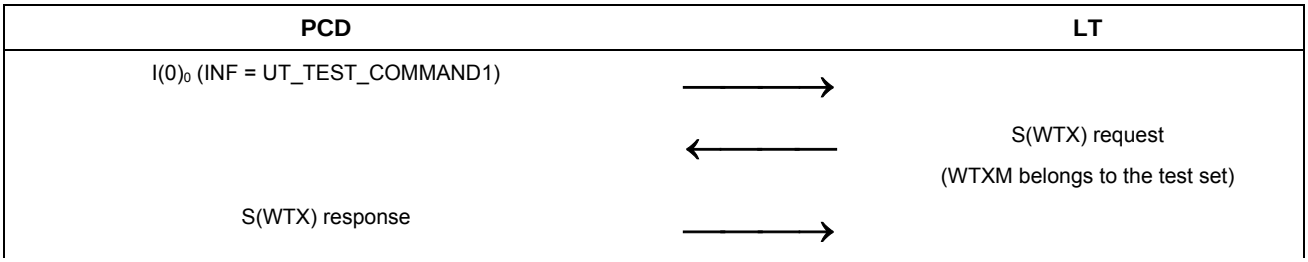
i) The LT waits until the PCD sends an I-block to the LT with the INF field containing the UT_TEST_COMMAND1. The PCD shall reset the FWT at this point.

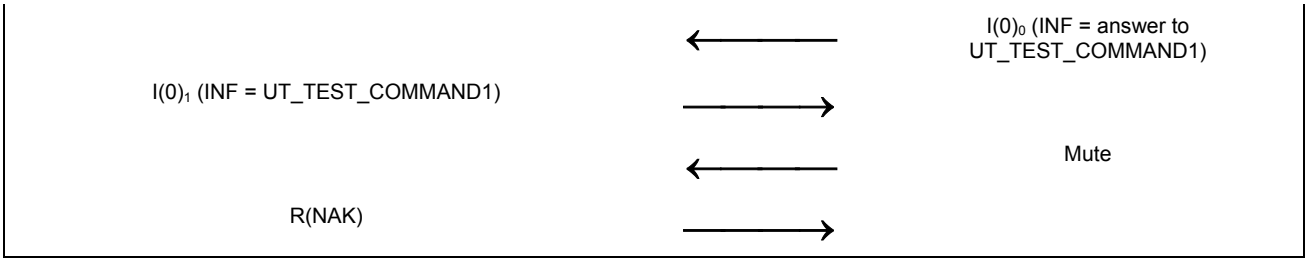
j) The LT remains Mute for at least the expected FWT. This fact means FWT timeout for the PCD.

k) Record the presence, the content and timing of the PCD-response. The PCD shall send an R(NAK) block only after FWT expires (ISO/IEC 14443-4:2001, 7.5.4.2).

l) Measure and record the time between the end of the PCD frame from step i) and start of PCD frame from step k).

Scenario H.18 —PCD reaction to the LT waiting time extension request, procedure 2





H.4.2.2.2.1 Expected result

The PCD command is expected according to the Scenario H.18 for all FWI and WTXM values defined in, H.4.2 in all combinations. The test shall pass only when every test with these different values passed.

H.4.2.2.2.2 Test report

Fill the appropriate row in Table H.11 — Reported Results for tests methods for both \ Type A and Type B according to Figure H.23 — Result criteria for Reaction of the PCD to request for waiting time extension Procedure 2 (ISO/IEC 14443-4:2001, 7.3):

Explanation	Test result
Only when the answer to TEST_COMMAND_1 was not sent back to the UT or when the PCD sent the R(NAK) before FWT expired	Fail
In any other case	Pass

Figure H.23 — Result criteria for Reaction of the PCD to request for waiting time extension Procedure 2 (ISO/IEC 14443-4:2001, 7.3)

H.4.3 Error detection and recovery

The purpose of this test is to determine the behaviour of PCD when an error occurs according to ISO/IEC 14443-4:2001, 7.5.5.

NOTE In this section, "Erroneous block" is a frame with a bad CRC.

H.4.3.1 Apparatus

See H.1.

H.4.3.2 Procedure

Place the LT into the PCD operating volume.

During the following procedure the RF Input/Receive data shall be continuously monitored and verified correct to ISO/IEC 14443-2:2001. All signal transitions (level and timing) as well as the logical content of the communication shall be recorded.

The UT performs the protocol activation procedure according to H.1.8.2 for Type A or H.1.8.3 for Type B.

H.4.3.2.1 Procedure 1 (ISO/IEC 14443-4:2001, Informative Annex B, Scenario 8)

Use the following sequence immediately after procedure H.4.3.2:

a) The UT sends the SEND_UT_APDU(UT_TEST_COMMAND1) to the PCD.

b) The LT waits until the PCD sends an I-block to the LT with the INF field containing the UT_TEST_COMMAND1.

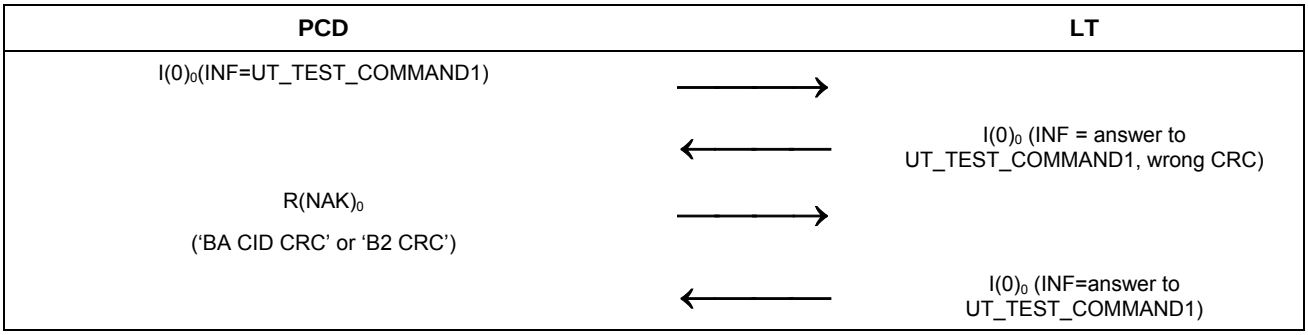
c) The LT sends an erroneous I-block to the PCD.

d) The PCD shall send $R(NAK)_0$.

e) The LT sends I-block (containing some response UT_APDU with answer to the UT_TEST_COMMAND1) to the PCD.

f) The PCD is expected to transfer the response UT_APDU back to the UT. Check at the UT that this response UT_APDU block is correctly accepted.

Scenario H.19 — Error detection and recovery of a transmission error by the PCD (ISO/IEC 14443-4:2001, Informative Annex B, Scenario 8), procedure 1



H.4.3.2.1.1 Expected result

The PCD's behaviour shall match the expected Test Scenario H.19 exactly.

H.4.3.2.1.2 Test report

Fill the appropriate row in Table H.11 — Reported Results for tests methods for both Type A and Type B according to Figure H.24 — Results criteria for Error detection and recovery Procedure 1 (ISO/IEC 14443-4:2001, Informative Annex B, Scenario 8):

Explanation	Test result
Only when the PCD's behaviour matches the expected Test Scenario exactly	Pass
When the PCD fails on any step of the Test Scenario	Fail

Figure H.24 — Results criteria for Error detection and recovery Procedure 1 (ISO/IEC 14443-4:2001, Informative Annex B, Scenario 8)

H.4.3.2.2 Procedure 2 (ISO/IEC 14443-4:2001, 7.5.4.2 rule 4)

Use the following sequence immediately after procedure H.4.3.2:

a) The UT sends the SEND_UT_APDU(UT_TEST_COMMAND1) to the PCD.

b) The LT waits until the PCD sends an I-block to the LT with the INF field containing the UT_TEST_COMMAND1.

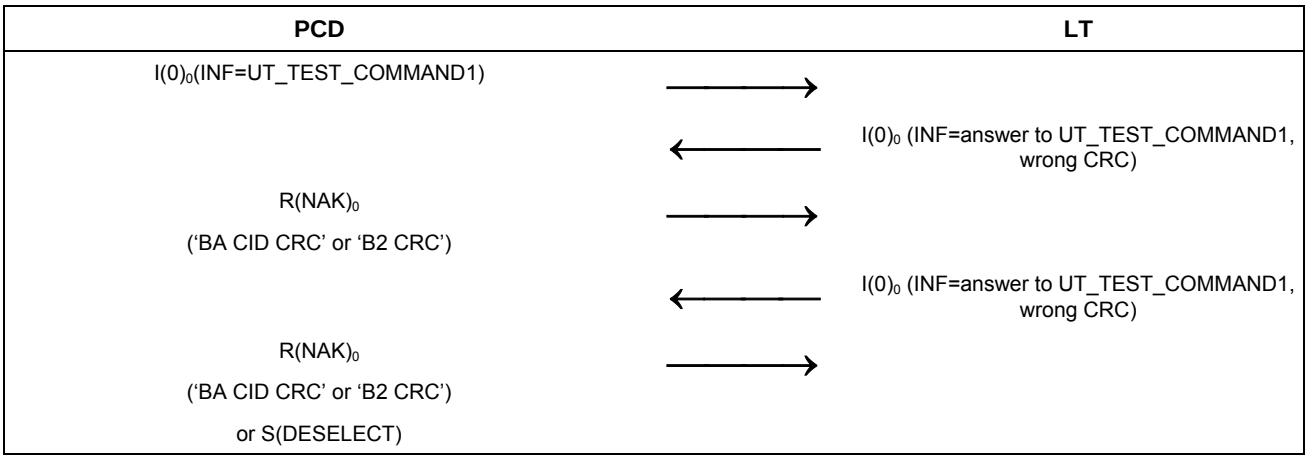
c) The LT sends an erroneous block to the PCD.

d) The PCD shall send $R(NAK)_0$.

e) The LT sends a second invalid block to the PCD.

f) The PCD shall send either $R(NAK)_0$ or S(DESELECT) request.

Scenario H.20 — Error detection and recovery of a transmission error by the PCD, Procedure 2



H.4.3.2.2.1 Expected result

The PCD's behaviour shall match the expected Test Scenario H.20 exactly.

H.4.3.2.2.2 Test report

Fill the appropriate row in Table H.11 — Reported Results for tests methods for both Type A and Type B according to Figure H.25 — Result criteria for Error detection and recovery Procedure 2 (ISO/IEC 14443-4:2001, 7.5.4.2 rule 4):

Explanation	Test result
Only when the PCD's behaviour matches the expected Test Scenario exactly	Pass
In any other case	Fail

Figure H.25 — Result criteria for Error detection and recovery Procedure 2 (ISO/IEC 14443-4:2001, 7.5.4.2 rule 4)

H.4.3.2.3 Procedure 3 (ISO/IEC 14443-4:2001, 7.5.4.2 rule 4)

Use the following sequence immediately after procedure H.4.3.2:

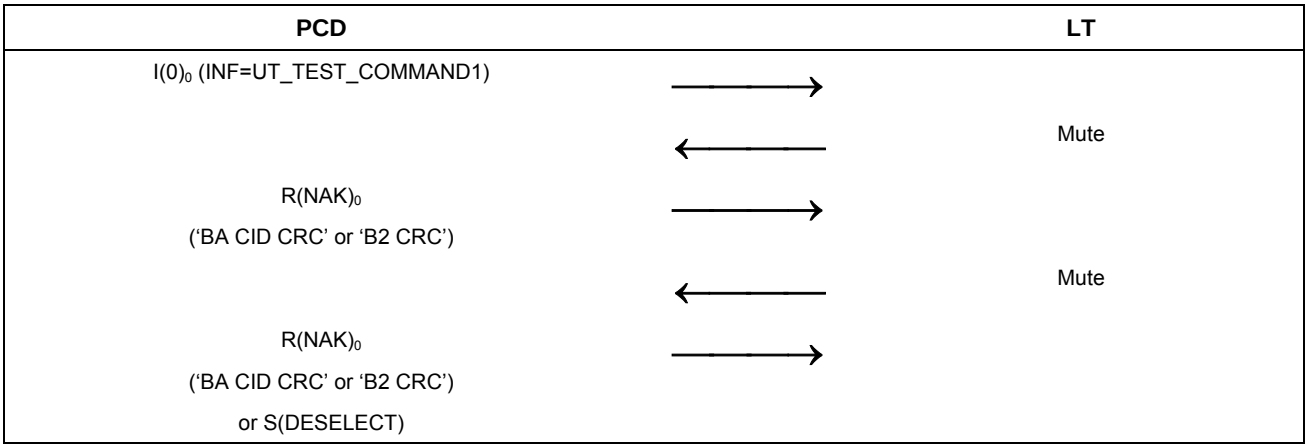
a) The UT sends the SEND_UT_APDU(UT_TEST_COMMAND1) to the PCD.

b) The LT waits until the PCD sends an I-block to the LT with the INF field containing the UT_TEST_COMMAND1.

c) Maintain the LT Mute.

d) Record all responses from the PCD. The PCD shall send $R(NAK)_0$ at least once.

Scenario H.21 — Recovery of a transmission error by the PCD, Procedure 3



H.4.3.2.3.1 Expected result

The PCD command is expected according to the Scenario H.21.

H.4.3.2.3.2 Test report

Fill the appropriate row in Table H.10 — Test coverage report for both Type A and Type B according to Figure H.26 — Result criteria for Error detection and recovery Procedure 3 (ISO/IEC 14443-4:2001, 7.5.4.2 rule 4):

Explanation	Test result
Only when the PCD sends $R(NAK)_0$ at least once	Pass
In any other case	Fail

Figure H.26 — Result criteria for Error detection and recovery Procedure 3 (ISO/IEC 14443-4:2001, 7.5.4.2 rule 4)

H.4.3.2.4 Procedure 4 (ISO/IEC 14443-4:2001, 7.5.4.2 rule 7)

Use the following sequence immediately after procedure H.4.3.2:

a) The UT sends the SEND_UT_APDU(UT_TEST_COMMAND1) to the PCD.

b) The LT waits until the PCD sends an I-block to the LT with the INF field containing the UT_TEST_COMMAND1.

c) The LT sends $R(ACK)_0$ (because of infringement of protocol rules by the LT).

d) The PCD shall send an S(DESELECT) request.

Scenario H.22 — Recovery of a protocol error by the PCD, Procedure 4

PCD		LT
$I(0)_0$ (INF=UT_TEST_COMMAND1)	→	
	←	$R(ACK)_0$ ('AA CID CRC' or 'A2 CRC') [a]
S(DESELECT) request	→	

[a] If the PCD block contains a CID, the left option shall be used, else the right option shall be used.

H.4.3.2.4.1 Expected result

The PCD command is expected according to the Scenario H.22.

H.4.3.2.4.2 Test report

Fill the appropriate row in Table H.11 — Reported Results for tests methods according to the test results both for Type A and Type B according to Figure H.27 — Result criteria for Error detection and recovery Procedure 4 (ISO/IEC 14443-4:2001, 7.5.4.2 rule 7):

Explanation	Test result
Only when the PCD sends a S(DESELECT) request (since $R(ACK)_0$ is an infringement of the protocol rules in this situation)	Pass
In any other case	Fail

Figure H.27 — Result criteria for Error detection and recovery Procedure 4 (ISO/IEC 14443-4:2001, 7.5.4.2 rule 7)

H.4.3.2.5 Procedure 5 (with chaining) (ISO/IEC 14443-4:2001, 7.5.4.2 rule 5, ISO/IEC 14443-4:2001, Informative Annex B, Scenario 19)

Use the following sequence immediately after procedure H.4.3.2:

a) The UT sends the SEND_UT_APDU(UT_TEST_COMMAND1) to the PCD.

b) The LT waits until the PCD sends an I-block to the LT, with the INF field containing the UT_TEST_COMMAND1.

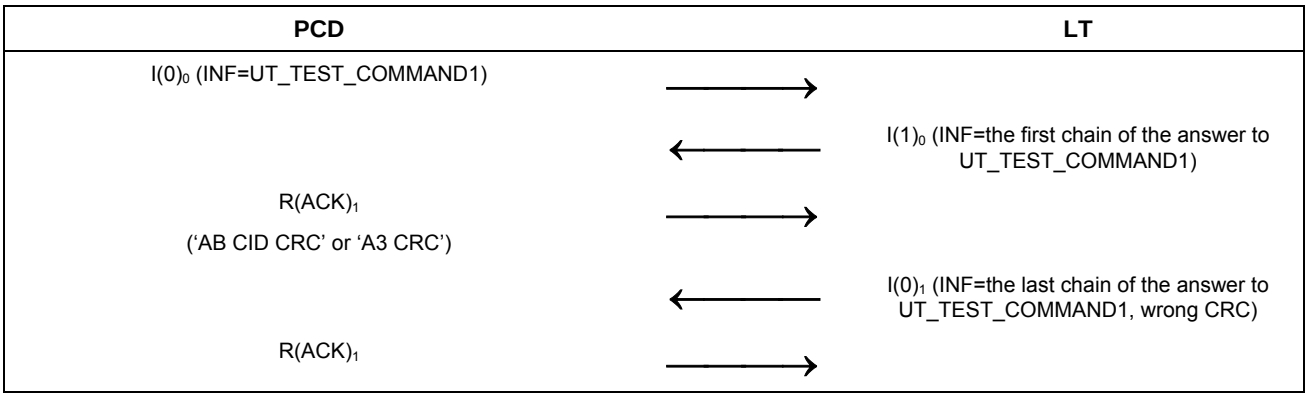
c) The LT sends the first block $I(1)_0$ of the chain and waits for the PCD response.

d) The PCD shall send $R(ACK)_1$.

e) The LT sends an erroneous block $I(0)_1$ to the PCD.

f) The PCD shall send $R(ACK)_1$.

Scenario H.23 — Recovery of a transmission error by the PCD, Procedure 5 (ISO/IEC 14443-4:2001, Informative Annex B, Scenario 19)



H.4.3.2.5.1 Expected result

The PCD command is expected according to the Scenario H.23.

H.4.3.2.5.2 Test report

Fill the appropriate row in Table H.11 — Reported Results for tests methods for both Type A and Type B according to Figure H.28 — Result criteria for Error detection and recovery Procedure 5 (with chaining) (ISO/IEC 14443-4:2001, 7.5.4.2 rule 5, ISO/IEC 14443-4:2001, Informative Annex B, Scenario 19):

Explanation	Test result
Only when the PCD's behaviour matches the expected Test Scenario exactly	Pass
In any other case	Fail

Figure H.28 — Result criteria for Error detection and recovery Procedure 5 (with chaining) (ISO/IEC 14443-4:2001, 7.5.4.2 rule 5, ISO/IEC 14443-4:2001, Informative Annex B, Scenario 19)

H.4.3.2.6 Procedure 6 (ISO/IEC 14443-4:2001, 7.5.4.2)

Use the following sequence immediately after procedure H.4.3.2:

a) The UT sends the SEND_UT_APDU(UT_TEST_COMMAND1) to the PCD.

b) The LT waits until the PCD sends an I-block to the LT with the INF field containing the UT_TEST_COMMAND1.

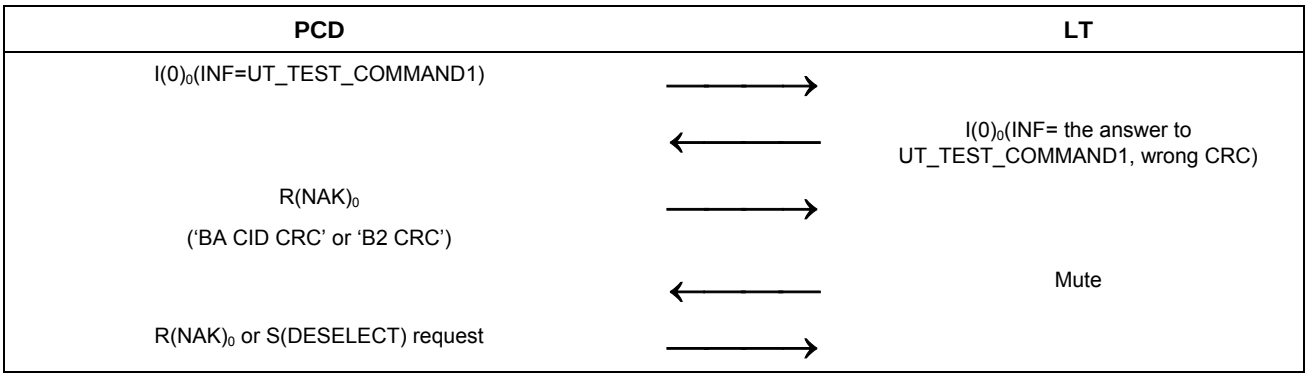
c) The LT sends an erroneous block to the PCD.

d) The PCD shall send $R(NAK)_0$.

e) The LT remains Mute.

f) Record all responses from the PCD. The PCD shall send either $R(NAK)_0$ or S(DESELECT).

Scenario H.24 — Recovery of a transmission error by the PCD, Procedure 6



H.4.3.2.6.1 Expected result

The PCD command is expected according to the Scenario H.24.

H.4.3.2.6.2 Test report

Fill the appropriate row in Table H.11 — Reported Results for tests methods for both Type A and Type B according to Figure H.29 — Result criteria for Error detection and recovery Procedure 6 (ISO/IEC 14443-4:2001, 7.5.4.2):

Explanation	Test result
Only when the PCD either sends $R(NAK)_0$ or S(DESELECT) request	Pass
In any other case	Fail

Figure H.29 — Result criteria for Error detection and recovery Procedure 6 (ISO/IEC 14443-4:2001, 7.5.4.2)

H.4.3.2.7 Procedure 7 (ISO/IEC 14443-4:2001, 7.5.5, Informative Annex B, Scenario 10)

Use the following sequence immediately after procedure H.4.3.2:

a) The UT sends the SEND_UT_APDU(UT_TEST_COMMAND1) to the PCD.

b) The LT waits until the PCD sends an I-block to the LT with the INF field containing the UT_TEST_COMMAND1.

c) The LT sends an erroneous S(WTX) request block.

d) The PCD shall send $R(NAK)_0$.

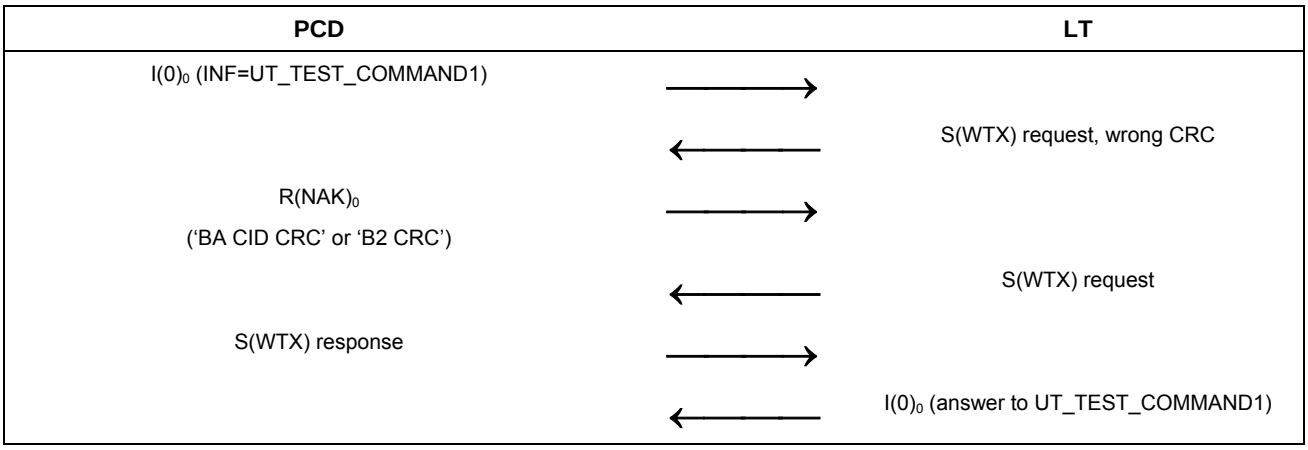
e) The LT sends a valid S(WTX) request block.

f) The PCD shall answer with S(WTX) response.

g) The LT sends I-block (containing some response UT_APDU with answer to the UT_TEST_COMMAND1) to the PCD.

h) The PCD is expected to transfer this response UT_APDU back to the UT. Check at the UT that this response UT_APDU block is correctly accepted.

Scenario H.25 — Recovery of a transmission error by the PCD, Procedure 7 (ISO/IEC 14443-4:2001, Informative Annex B, Scenario 10)



H.4.3.2.7.1 Expected result

The PCD's behaviour shall match the expected Test Scenario H.25 exactly.

H.4.3.2.7.2 Test report

Fill the appropriate row in Table H.11 — Reported Results for tests methods for both Type A and Type B Figure H.30 — Result criteria for Error detection and recovery Procedure 7 (ISO/IEC 14443-4:2001, 7.5.5, Informative Annex B, Scenario 10):

Explanation	Test result
Only when the PCD's behaviour matches the expected Test Scenario exactly	Pass
When the PCD failson any step of the Test Scenario	Fail

Figure H.30 — Result criteria for Error detection and recovery Procedure 7 (ISO/IEC 14443-4:2001, 7.5.5, Informative Annex B, Scenario 10)

H.4.3.2.8 Procedure 8 (ISO/IEC 14443-4:2001, 7.5.5, Informative Annex B, Scenario 13)

Use the following sequence immediately after procedure H.4.3.2:

a) The UT sends the SEND_UT_APDU(UT_TEST_COMMAND1) to the PCD.

b) The LT waits until the PCD sends an I-block to the LT with the INF field containing the UT_TEST_COMMAND1.

c) The LT sends an S(WTX) request block.

d) The PCD shall answer with S(WTX) response.

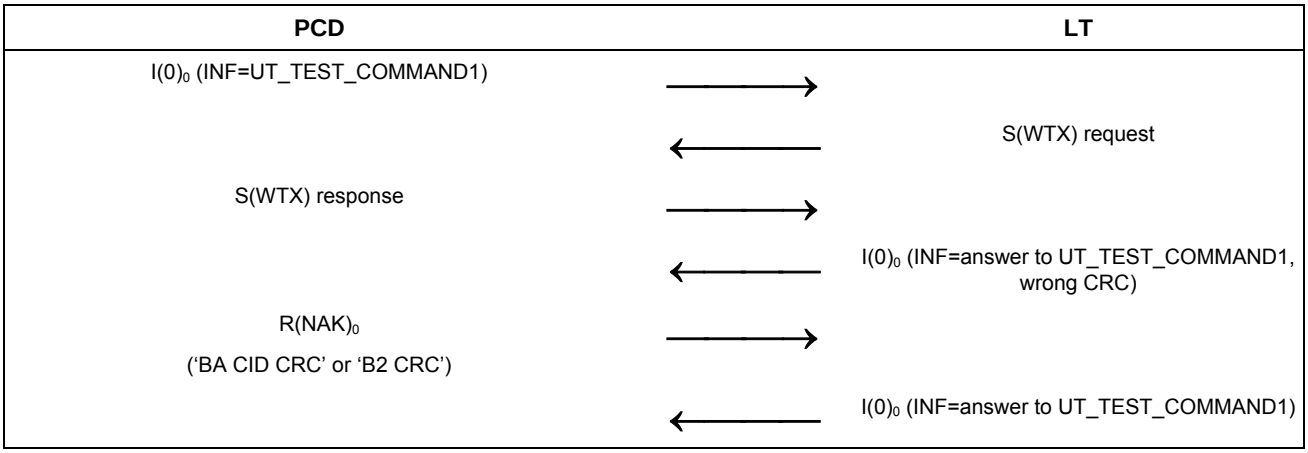
e) The LT sends an erroneous $I(0)_0$ block.

f) The PCD shall send $R(NAK)_0$.

g) The LT sends a valid $I(0)_0$ block with maximum timing between $R(NAK)_0$ and $I(0)_0$ to check that the PCD FWT is still extended.

h) The PCD is expected to transfer this response UT_APDU back to the UT. Check at the UT that this response UT_APDU block is correctly accepted.

Scenario H.26 — Recovery of a transmission error by the PCD, Procedure 8 (ISO/IEC 14443-4:2001, Informative Annex B, Scenario 13)



H.4.3.2.8.1 Expected result

The PCD's behaviour shall match the expected Test Scenario H.26 exactly.

H.4.3.2.8.2 Test report

Fill the appropriate row in Table H.11 — Reported Results for tests methods for both Type A and Type B according to Figure H.31 — Result criteria for Error detection and recovery Procedure 8 (ISO/IEC 14443-4:2001, 7.5.5, Informative Annex B, Scenario 13):

Explanation	Test result
If the PCD's behaviour matches the expected Test Scenario exactly	Pass
If the PCD fails even on one step of the Test Scenario	Fail

Figure H.31 — Result criteria for Error detection and recovery Procedure 8 (ISO/IEC 14443-4:2001, 7.5.5, Informative Annex B, Scenario 13)

H.4.3.2.9 Procedure 9 (with chaining) (see ISO/IEC 14443-4:2001, Informative Annex B, Scenario 16)

Use the following sequence immediately after procedure H.4.3.2:

a) The UT sends the SEND_UT_APDU(UT_TEST_COMMAND2(causing 3 chains)) to the PCD.

b) The LT waits until the PCD sends an I-block $I(1)_0$ to the LT, with the INF field the first chain of the UT_TEST_COMMAND2.

c) The LT sends an erroneous $R(ACK)_0$.

d) The PCD shall send $R(NAK)_0$.

e) The LT sends $R(ACK)_0$.

f) The PCD shall send the next block $I(1)_1$ of the chain.

g) The LT sends $R(ACK)_1$.

h) The PCD shall send the last block $I(0)_0$ of the chain .

i) The LT sends I-block (containing some response UT_APDU with answer to the UT_TEST_COMMAND2) to the PCD.

j) The PCD is expected to transfer this response UT_APDU back to the UT. Check at the UT that this response UT_APDU block is correctly accepted.

NOTE In case the number of chains cannot be controlled exactly, modify the expected procedure to reflect the test purpose which is to make sure that the block numbering and the chaining are properly executed after transmission error at step c).

Scenario H.27 — Recovery of a transmission error by the PCD, Procedure 9 (with chaining) (ISO/IEC 14443-4:2001, Informative Annex B, Scenario 16)

PCD		LT
$I(1)_0$ (INF = the first chain of the UT_TEST_COMMAND2)	→	
	←	$R(ACK)_0$, wrong CRC ('AA CID 00 00' or 'A2 00 00') [a]
$R(NAK)_0$ ('BA CID CRC' or 'B2 CRC')	→	
	←	$R(ACK)_0$ ('AA CID CRC' or 'A2 CRC') [a]
$I(1)_1$ (INF = the second chain of the UT_TEST_COMMAND2)	→	
	←	$R(ACK)_1$ ('AB CID CRC' or 'A3 CRC') [a]
$I(0)_0$ (INF = the last chain of the UT_TEST_COMMAND2)	→	
	←	$I(0)_0$ (INF=the answer to UT_TEST_COMMAND2)

[a] If the PCD frame contains a CID, the left option shall be used, else the right option shall be used.

H.4.3.2.9.1 Expected result

The PCD's behaviour shall be in accordance with Scenario H.27.

H.4.3.2.9.2 Test report

Fill the appropriate row in "Table H.11 — Reported Results for tests methods" for both Type A and Type B according to Figure H.32 — Result criteria for Error detection and recovery Procedure 9 (with chaining) (see ISO/IEC 14443-4:2001, Informative Annex B, Scenario 16):

Explanation	Test result
Only when the PCD's behaviour matches	Pass

the expected Test Scenario	
When the PCD fails on any step of the Test Scenario	Fail

Figure H.32 — Result criteria for Error detection and recovery Procedure 9 (with chaining) (see ISO/IEC 14443-4:2001, Informative Annex B, Scenario 16)

H.4.3.2.10 Procedure 10 (with chaining) (see ISO/IEC 14443-4:2001, Informative Annex B, Scenario 17)

Use the following sequence immediately after procedure H.4.3.2:

a) The UT sends the SEND_UT_APDU(UT_TEST_COMMAND2(causing 3 chains)) to the PCD.

b) The LT waits until the PCD sends an I-block $I(1)_0$ to the LT, with the INF field the first chain of the UT_TEST_COMMAND2.

c) The LT remains Mute.

d) The PCD shall send $R(NAK)_0$.

e) The LT sends a R-block with a not synchronized sequential block number $R(ACK)_1$.

f) The PCD shall repeat the previous I-block $I(1)_0$ to the LT .

g) The LT sends $R(ACK)_0$.

h) The PCD shall send the next block $I(1)_1$ of the chain.

i) The LT sends $R(ACK)_1$.

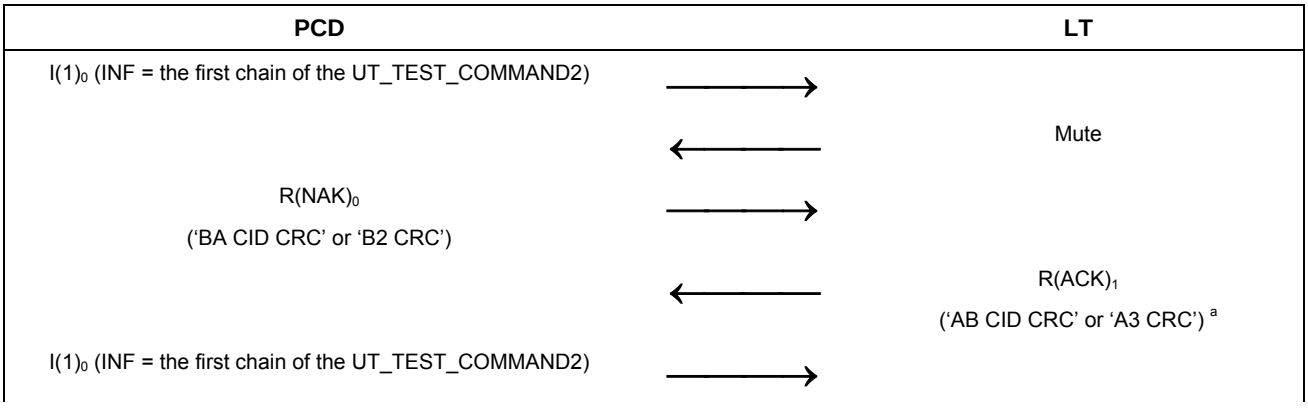
j) The PCD shall send the last block $I(0)_0$ of the chain.

k) The LT sends I-block (containing some response UT_APDU with answer to the UT_TEST_COMMAND2) to the PCD.

l) The PCD is expected to transfer this response UT_APDU back to the UT. Check at the UT that this response UT_APDU block is correctly accepted.

NOTE In case the number of chains cannot be controlled exactly, modify the expected procedure to reflect the test purpose which is to make sure that the block numbering and the chaining are properly executed after Mute at step c).

Scenario H.28 — Recovery of a transmission error by the PCD, Procedure 10 (with chaining) (see ISO/IEC 14443-4:2001, Informative Annex B, Scenario 17)



PCD		LT
	←	$R(ACK)_0$ ('AA CID CRC' or 'A2 CRC') [a]
$I(1)_1$ (INF = the second chain of the UT_TEST_COMMAND2)	→	
	←	$R(ACK)_1$ ('AB CID CRC' or 'A3 CRC') [a]
$I(0)_0$ (INF = the last chain of the UT_TEST_COMMAND2)	→	
	←	$I(0)_0$ (INF=the answer to UT_TEST_COMMAND2)

[a] If the PCD block contains a CID, the left option shall be used, else the right option shall be used.

H.4.3.2.10.1 Expected result

The PCD's behaviour shall match the expected Test Scenario H.28 exactly.

H.4.3.2.10.2 Test report

Fill the appropriate row in Table H.11 — Reported Results for tests methods for both Type A and Type B according to Figure H.33 — Result criteria for Error detection and recovery Procedure 10 (with chaining) (see ISO/IEC 14443-4:2001, Informative Annex B, Scenario 17):

Explanation	Test result
Only when the PCD's behaviour matches the expected Test Scenario exactly	Pass
When the PCD fails on any step of the Test Scenario	Fail

Figure H.33 — Result criteria for Error detection and recovery Procedure 10 (with chaining) (see ISO/IEC 14443-4:2001, Informative Annex B, Scenario 17)

H.4.3.2.11 Procedure 11 (with chaining) (see ISO/IEC 14443-4:2001, Informative Annex B, Scenario 20)

Use the following sequence immediately after procedure H.4.3.2:

a) The UT sends the SEND_UT_APDU(UT_TEST_COMMAND1) to the PCD.

b) The LT waits until the PCD sends an I-block $I(0)_0$ to the LT, with the INF field containing the UT_TEST_COMMAND1.

c) The LT sends I-block $I(1)_0$ indicating chaining.

d) The PCD shall send $R(ACK)_1$.

e) The LT sends erroneous I-block $I(1)_1$ to the PCD.

f) The PCD shall send $R(ACK)_1$.

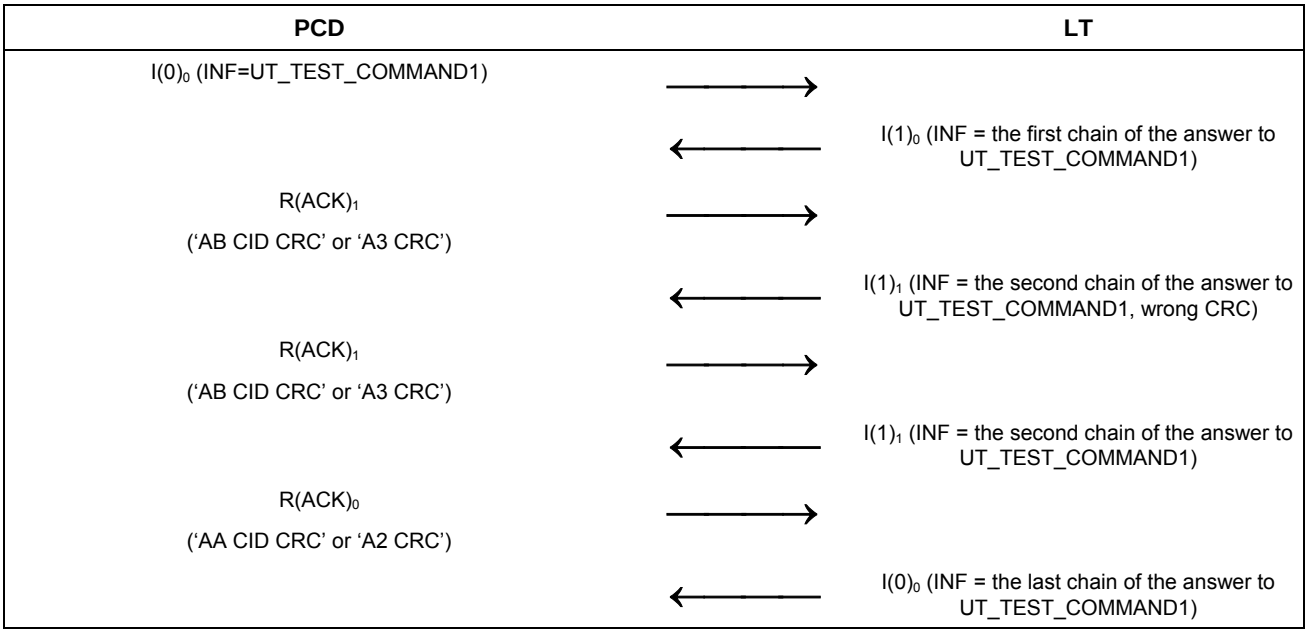
g) The LT retransmits an I-block $I(1)_1$ without error.

h) The PCD shall send $R(ACK)_0$.

i) The LT sends the last block of the chain in I-block $I(0)_0$ (of its response UT_APDU with answer to the UT_TEST_COMMAND1) to the PCD.

j) The PCD is expected to transfer the response UT_APDU, containing all chaining segments, back to the UT. Check at the UT that this response UT_APDU block is correctly accepted.

Scenario H.29 — Recovery of a transmission error by the PCD, Procedure 11 (with chaining) (ISO/IEC 14443-4:2001, Informative Annex B, Scenario 20)



H.4.3.2.11.1 Expected result

The PCD's behaviour shall in accordance with Scenario H.29 exactly.

H.4.3.2.11.2 Test report

Fill the appropriate row in Table H.11 — Reported Results for tests methods for both Type A and Type B according to Figure H.34 — Result criteria for Error detection and recovery Procedure 11 (with chaining) (see ISO/IEC 14443-4:2001, Informative Annex B, Scenario 20):

Explanation	Test result
Only when the PCD's behaviour matches the expected Test Scenario exactly	Pass
When the PCD fails on any step of the Test Scenario	Fail

Figure H.34 — Result criteria for Error detection and recovery Procedure 11 (with chaining) (see ISO/IEC 14443-4:2001, Informative Annex B, Scenario 20)

H.4.3.2.12 Procedure 12 (ISO/IEC 14443-4:2001, 7.5.4.2 rule 8)

Use the following sequence immediately after procedure H.4.3.2:

a) The UT sends the SEND_UT_APDU(UT_TEST_COMMAND1) to the PCD.

b) The LT waits until the PCD sends an I-block to the LT with the INF field containing the UT_TEST_COMMAND1.

c) The LT remains Mute.

d) The LT waits until the PCD sends $R(NAK)_0$ block (R-block may be sent more than once).

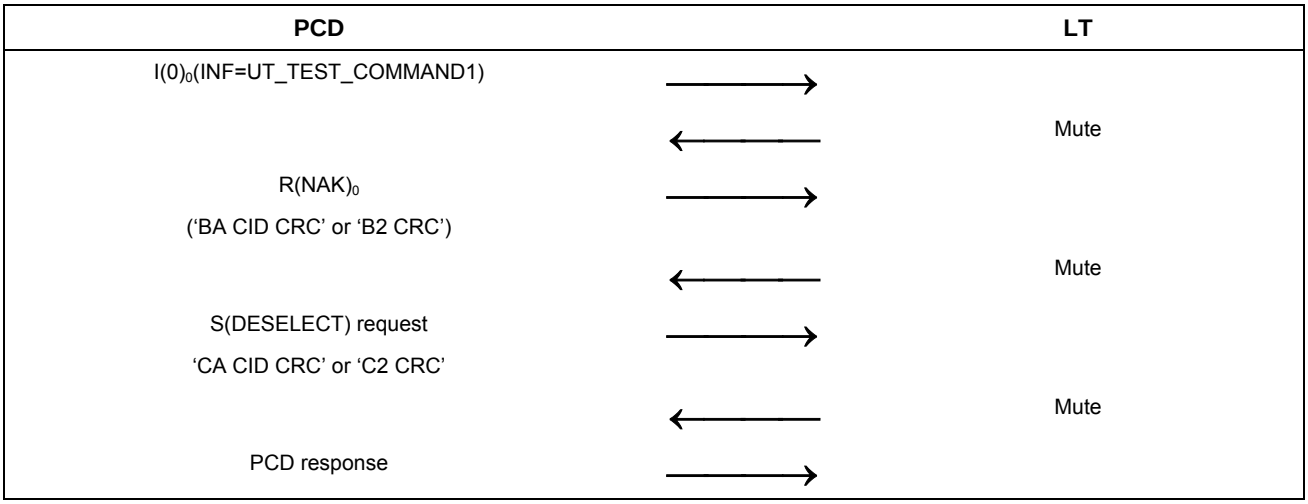
e) The LT remains Mute.

f) The LT waits until the PCD sends a S(DESELECT) request block to the LT.

g) The LT remains Mute.

h) Record the response from the PCD. The PCD may retransmit the S(DESELECT) request block.

Scenario H.30 — Recovery of a transmission error by the PCD, Procedure 12



H.4.3.2.12.1 Expected result

The PCD command is expected according to the Scenario H.30.

H.4.3.2.12.2 Test report

Fill the appropriate row in Table H.11 — Reported Results for tests methods for both Type A and Type B according to Figure H.35 — Result criteria for Error detection and recovery Procedure 12 (ISO/IEC 14443-4:2001, 7.5.4.2 rule 8):

Explanation	Test result
Only when the PCD retransmits the S(DESELECT) or ignores the LT	Pass
In any other case	Fail

Figure H.35 — Result criteria for Error detection and recovery Procedure 12 (ISO/IEC 14443-4:2001, 7.5.4.2 rule 8)

H.4.4 Handling of NAD during chaining

The purpose of this test is to ensure that the PCD maintains NAD in the proper way.

H.4.4.1 Apparatus

See H.1.

H.4.4.2 Procedure

During the following procedure the logical content of the communication shall be recorded.

a) Place the LT into the PCD operating volume.

b) Configure the LT as one supporting NAD.

c) Repeat procedure from Scenario H.27.

H.4.4.3 Expected result

NAD shall only be present in the first packet of chaining if used.

H.4.4.4 Test report

Fill the appropriate rows in Table H.11 — Reported Results for tests methods for both Type A and Type B according to Figure H.36 — Result criteria for Handling of NAD during chaining:

Explanation	Test result
Only when the PCD use the NAD only in the first packet of chaining or does not use NAD.	Pass
In any other case	Fail

Figure H.36 — Result criteria for Handling of NAD during chaining

H.5 Continuous monitoring of packets sent by the PCD

The purpose of this test is to ensure that the PCD does not set any RFU bits in any sent frame to any value other than the default value documented for such RFU bit. Further, the test shall also ensure that no field is ever set to RFU value. The test shall also ensure that the R-block and the S-block match the protocol definitions. And that rules given regarding the first byte of the packet are not violated.

H.5.1 RFU fields

RFU fields shall be continuously monitored during the testing and shall always be verified to contain the assigned default value. A test shall fail and the tested PCD declared non-compliant in case an RFU field is not set to its default value at any time.

H.5.2 RFU values

Functional fields shall be continuously monitored during the testing and shall always be verified to contain only functional values documented in the standard or proprietary values documented as such in the standard. A test shall fail and the tested PCD be declared non-compliant in case a functional field is not set to said values at any time.

H.5.3 R-block

R-block shall never contain an INF field (see ISO/IEC 14443-4:2001, 7.1.1.1).

H.5.4 S-block

S-block shall have an INF field of one byte only when it is a WTX block and no INF field otherwise (see ISO/IEC 14443-4:2001, 7.1.1.1).

H.5.5 PCB

PCB byte shall contain allowed values, (see ISO/IEC 14443-4:2001, 7.1.1.1 and ISO/IEC 14443-4:2001, Annex C).

H.5.6 Short Frame

Short frame (Type A only) shall contain allowed values, (see ISO/IEC 14443-3:2001, 6.3.1 and 6.4.3.2).

H.5.7 Apparatus

See H.1.

H.5.8 Procedure

During all test procedures and scenarios the logical content of the communication shall always be recorded.

H.5.9 Test report

Fill the appropriate row in Table H.11 — Reported Results for tests methods according Figure H.37 — Result criteria for Continuous monitoring of packets sent by the PCD:

Explanation	Test result
Only when the PCD does not set RFU bits to values other than default in all sent frames and never sets any field to RFU value and does not violate the length rules of R-block, S-block and first byte coding of Block and Frame (as informatively summarized in Annex C of ISO/IEC 14443-4:2001)	Pass
When the PCD sets any RFU bit to a value other than the default value in any sent frames or sets any field to an RFU value or violates the length rules of R-block or S-block or violates the first byte rules coding of Block and Frame (as informatively summarized in Annex C of ISO/IEC 14443-4:2001)	Fail

Figure H.37 — Result criteria for Continuous monitoring of packets sent by the PCD

H.6 Reported results

Table H.5 — Type A Specific Timing table

No	Parameter	ISO Reference	Reference value	Measured value
1	Frame delay time PICC to PCD	ISO/IEC 14443-3:2001, 6.1.3	at least 1172/fc (~ 86 µs)	
2	Request Guard Time	ISO/IEC 14443-3:2001, 6.1.4	at least 7000/fc (~ 512 µs)	

NOTE All timing values are calculated for carrier frequency *fc* = 13,56 MHz and bit rate *fc*/128 (~106 kbit/s).

Table H.6 — Type B Specific Timing table

No	Parameter	ISO Reference	Minimum	Maximum	Measured value
1	SOF low	ISO/IEC 14443-3:2001, 7.1.4	10 etu (~94,40 µs)	11 etu (~103,83 µs)	
2	EOF low	ISO/IEC 14443-3:2001, 7.1.5	10 etu (~94,40 µs)	11 etu (~103,83 µs)	
3	Bit boundaries	ISO/IEC 14443-3:2001, 7.1.1	(n – 0,125) etu	(n + 0,125) etu	
4	EGT PCD to PICC	ISO/IEC 14443-3:2001, 7.1.2	0 µs	57 µs	
5	Minimum delay between the PICC EOF start and PCD SOF start	ISO/IEC 14443-3:2001, 7.1.7	10 etu + 32/*fs*	No maximum	

NOTE All timing values are calculated for carrier frequency *fc* = 13,56 MHz and bit rate *fc*/128 (~106 kbit/s).

Table H.7 — Reported Results for Type A specific test methods

Test method from ISO/IEC 10373-6		Scenario Numbers		Test result
Clause	Parameter	Test Scenario Number ISO/IEC 10373-6	Scenario Number ISO/IEC 14443-4:2001, Informative Annex B	PASS or FAIL or N/A [a]
H.2.1	Frame delay time PICC to PCD			
H.2.2	Request Guard Time			
H.2.3	Handling of bit collision during ATQA			
H.2.4	Handling of anticollision loop	Scenario H.1		
		Scenario H.2		
		Scenario H.3		
		Scenario H.4		
H.2.5	Handling of RATS and ATS	Scenario H.6		

		Scenario H.7		
		Scenario H.8		
H.2.6	Handling of PPS response	Scenario H.9		
		Scenario H.10		
H.2.7	Frame size selection mechanism	Scenario H.11		
H.2.8	Handling of Start-up Frame Guard Time	Scenario H.12		
H.2.9	Handling of the CID during activation by the PCD	Scenario H.13		
[a] In case a test has several procedures indicate PASS only in case every individual procedure is PASS.				

Table H.9 — Reported Results for Type B specific tests methods

Test method from ISO/IEC 10373-6		Scenario Numbers		Test result
Clause	Parameter	Test Scenario Number ISO/IEC 10373-6	Scenario Number ISO/IEC 14443-4:2001, Informative Annex B	PASS or FAIL [a]
H.3.1	I/O transmission timing			
H.3.2	Frame size selection mechanism	Scenario H.14		
H.3.3	Handling of the CID during activation by the PCD	Scenario H.15		
		Scenario H.16		
[a] In case a test has several procedures indicate PASS only in case every individual procedure is PASS.				

Table H.11 — Reported Results for tests methods

Test method from ISO/IEC 10373-6		Scenario Numbers		Test result	
Clause	Parameter	Test Scenario Number ISO/IEC 10373-6	Scenario Number ISO/IEC 14443-4:2001, Informative Annex B	**Type A** [a]	**Type B** [a]
H.4.1	Handling of the polling loop				
H.4.2	Reaction of the PCD to request for waiting time extension	Scenario H.17			
		Scenario H.18			
H.4.3	Error detection and recovery	Scenario H.19	Scenario 8 "Exchange of I-blocks"		

		Scenario H.20			
		Scenario H.21			
		Scenario H.22			
		Scenario H.23	Scenario 19 "PICC uses chaning"		
		Scenario H.24			
		Scenario H.25	Scenario 10 "Request for waiting time extension"		
		Scenario H.26	Scenario 13 "Request for waiting time extension"		
		Scenario H.27	Scenario 16 "PCD uses chaining"		
		Scenario H.28	Scenario 17 "PCD uses chaining"		
		Scenario H.29	Scenario 20 "PICC uses chaining"		
		Scenario H.30			
H.4.4	Handling of NAD during chaining				
H.5	Continuous monitoring of packets sent by the PCD				

[a] In case a test has several procedures, indicate PASS only when every individual procedure is PASS.

Table H.10 — Test coverage report

No	Parameter	Description	Information
1	Chaining	Tested only if there is a command that supports more than 16 bytes	
2	NAD handling		

Table H.11 — PCD RFU table report

Name	PCD command	RFU field/value	Value		Test result
			Default	Not allowed	PASS or FAIL or Not Done
short frame Type A	REQA/WUPA	RFU values		All other values than '26' '52' '35' '40'-'4F' '78'-7F'	
SEL coding	SEL	RFU values (b4 to b1)		All other values than '93', '95', '97' and '92', '94', 98'	
AFI	REQB/WUPB	RFU values		All values from '90' up to 'FF'	
PARAM	REQB/WUPB	RFU field (b8 to b5)	(0000)b	All other values	
		RFU values in number of slots (b3 to b1)		(101)b (110)b (111)b	
PARAM1	ATTRIB	RFU field (b2 to b1)	(00)b	All other values	
Minimum TR0	ATTRIB	RFU values (b8 to b7)		(11)b	
Minimum TR1	ATTRIB	RFU values (b6 to b5)		(11)b	
PARAM2	ATTRIB	RFU values (b4 to b1)		All values from '9'((1001)b) up to 'F'((1111)b)	
PARAM3	ATTRIB	RFU field (b8 to b5)	(0000)b	All other values	
PARAM4	ATTRIB	RFU field (b8 to b5)	(0000)b	All other values	
PARAM4	ATTRIB	RFU value (b4 to b1)		'F'((1111)b)	

Annex I
(normative)

Removed

Annex J
(normative)

High bit rate selection test methods for PCD

J.1 Apparatus

In this test the PCD-test-apparatus shall be configurable to change the bit rate during the test procedure. Tester shall be able to measure the bit rate used by the PCD on each stage of this test procedure.

J.2 Procedure

Place the PCD-test-apparatus into the field of the PCD.

J.2.1 Procedure for Type A

The following procedure shall be repeated for all values of interface byte TA(1) defined in Table J.1 — Correct behaviour of PCD after ATS with TA(1):

a) Run through activation sequence as defined in ISO/IEC 14443-3.

b) The PCD shall send a RATS command as defined in ISO/IEC 14443-4.

c) The PCD-test-apparatus answers with a valid ATS including TA(1) according to Table J.1 — Correct behaviour of PCD after ATS with TA(1).

d) The PCD may optionally send a PPS with a valid parameter setting for PPS1 byte according to Table J.1 — Correct behaviour of PCD after ATS with TA(1).

e) If the PCD has sent a PPS then the PCD-test-apparatus acknowledges the received PPS with a valid PPS response.

f) The PCD shall send $I(0)_0$ block using the bit rate selected.

NOTE This block may also be $I(1)_0$, or R(NAK) in case of PICC presence check method 2a.

g) The PCD-test-apparatus sends a valid response using the bit rate selected. Check, if the answer from the PCD-test apparatus is accepted by the PCD.

NOTE The following steps may not be applicable when a PCD is embedded in a product:

h) The PCD shall send an S(DESELECT) request using the bit rate selected.

i) The PCD-test-apparatus sends a valid S(DESELECT) response using the bit rate selected. Check, if the answer from the PCD-test apparatus is accepted by the PCD.

j) The PCD shall send a valid REQA Command frame using the bit rate fc/128.

k) The PCD-test-apparatus answers with a valid ATQA.

Table J.1 — Correct behaviour of PCD after ATS with TA(1)

TA(1)	Valid parameter setting for PPS1
(10000000)b	(00000000)b [a]
(10010001)b	(00000101)b, (00000000)b
(10100010)b	(00001010)b, (00000000)b
(10110011)b	(00000101)b, (00001010)b, (00000000)b
(11000100)b	(00001111)b, (00000000)b
(11010101)b	(00000101)b, (00001111)b, (00000000)b
(11100110)b	(00001010)b, (00001111)b, (00000000)b
(11110111)b	(00000101)b, (00001010)b, (00001111)b, (00000000)b
(00000000)b	(00000000)b [a]
(00000001)b	(00000001)b, (00000000)b
(00000010)b	(00000010)b, (00000000)b
(00000011)b	(00000001)b, (00000010)b, (00000000)b
(00000100)b	(00000011)b, (00000000)b
(00000101)b	(00000001)b, (00000011)b, (00000000)b
(00000110)b	(00000010)b, (00000011)b, (00000000)b
(00000111)b	(00000001)b, (00000010)b, (00000011)b, (00000000)b
(00010000)b	(00000000)b (00000100)b
(00010001)b	(00000001)b, (00000000)b (00000101)b, (00000100)b
(00010010)b	(00000010)b, (00000000)b (00000110)b, (00000100)b
(00010011)b	(00000001)b, (00000010)b, (00000000)b (00000101)b, (00000110)b, (00000100)b
(00010100)b	(00000011)b, (00000000)b (00000111)b, (00000100)b
(00010101)b	(00000001)b, (00000011)b, (00000000)b (00000101)b, (00000111)b, (00000100)b
(00010110)b	(00000010)b, (00000011)b, (00000000)b (00000110)b, (00000111)b, (00000100)b
(00010111)b	(00000001)b, (00000010)b, (00000011)b, (00000000)b (00000101)b, (00000110)b, (00000111)b, (00000100)b
(00100000)b	(00000000)b (00001000)b
(00100001)b	(00000001)b, (00000000)b (00001001)b, (00001000)b
(00100010)b	(00000010)b, (00000000)b (00001010)b, (00001000)b
(00100011)b	(00000001)b, (00000010)b, (00000000)b (00001001)b, (00001010)b, (00001000)b
(00100100)b	(00000011)b, (00000000)b (00001011)b, (00001000)b

TA(1)	Valid parameter setting for PPS1
(00100101)b	(00000001)b, (00000011)b, (00000000)b (00001001)b, (00001011)b, (00001000)b
(00100110)b	(00000010)b, (00000011)b, (00000000)b (00001010)b, (00001011)b, (00001000)b
(00100111)b	(00000001)b, (00000010)b, (00000011)b, (00000000)b (00001001)b, (00001010)b, (00001011)b, (00001000)b
(00110000)b	(00000000)b (00000100)b (00001000)b
(00110001)b	(00000001)b, (00000000)b (00000101)b, (00000100)b (00001001)b, (00001000)b
(00110010)b	(00000010)b, (00000000)b (00000110)b, (00000100)b (00001010)b, (00001000)b
(00110011)b	(00000001)b, (00000010)b, (00000000)b (00000101)b, (00000110)b, (00000100)b (00001001)b, (00001010)b, (00001000)b
(00110100)b	(00000011)b, (00000000)b (00000111)b, (00000100)b (00001011)b, (00001000)b
(00110101)b	(00000001)b, (00000011)b, (00000000)b (00000101)b, (00000111)b, (00000100)b (00001001)b, (00001011)b, (00001000)b
(00110110)b	(00000010)b, (00000011)b, (00000000)b (00000110)b, (00000111)b, (00000100)b (00001010)b, (00001011)b, (00001000)b
(00110111)b	(00000001)b, (00000010)b, (00000011)b, (00000000)b (00000101)b, (00000110)b, (00000111)b, (00000100)b (00001001)b, (00001010)b, (00001011)b, (00001000)b
(01000000)b	(00000000)b (00001100)b
(01000001)b	(00000001)b, (00000000)b (00001101)b, (00001100)b
(01000010)b	(00000010)b, (00000000)b (00001110)b, (00001100)b
(01000011)b	(00000001)b, (00000010)b, (00000000)b (00001101)b, (00001110)b, (00001100)b
(01000100)b	(00000011)b, (00000000)b (00001111)b, (00001100)b
(01000101)b	(00000001)b, (00000011)b, (00000000)b (00001101)b, (00001111)b, (00001100)b
(01000110)b	(00000010)b, (00000011)b, (00000000)b (00001110)b, (00001111)b, (00001100)b
(01000111)b	(00000001)b, (00000010)b, (00000011)b, (00000000)b (00001101)b, (00001110)b, (00001111)b, (00001100)b
(01010000)b	(00000000)b (00000100)b (00001100)b

TA(1)	Valid parameter setting for PPS1
(01010001)b	(00000001)b, (00000000)b (00000101)b, (00000100)b (00001101)b, (00001100)b
(01010010)b	(00000010)b, (00000000)b (00000110)b, (00000100)b (00001110)b, (00001100)b
(01010011)b	(00000001)b, (00000010)b, (00000000)b (00000101)b, (00000110)b, (00000100)b (00001101)b, (00001110)b, (00001100)b
(01010100)b	(00000011)b, (00000000)b (00000111)b, (00000100)b (00001111)b, (00001100)b
(01010101)b	(00000001)b, (00000011)b, (00000000)b (00000101)b, (00000111)b, (00000100)b (00001101)b, (00001111)b, (00001100)b
(01010110)b	(00000010)b, (00000011)b, (00000000)b (00000110)b, (00000111)b, (00000100)b (00001110)b, (00001111)b, (00001100)b
(01010111)b	(00000001)b, (00000010)b, (00000011)b, (00000000)b (00000101)b, (00000110)b, (00000111)b, (00000100)b (00001101)b, (00001110)b, (00001111)b, (00001100)b
(01100000)b	(00000000)b (00001000)b (00001100)b
(01100001)b	(00000001)b, (00000000)b (00001001)b, (00001000)b (00001101)b, (00001100)b
(01100010)b	(00000010)b, (00000000)b (00001010)b, (00001000)b (00001110)b, (00001100)b
(01100011)b	(00000001)b, (00000010)b, (00000000)b (00001001)b, (00001010)b, (00001000)b (00001101)b, (00001110)b, (00001100)b
(01100100)b	(00000011)b, (00000000)b (00001011)b, (00001000)b (00001111)b, (00001100)b
(01100101)b	(00000001)b, (00000011)b, (00000000)b (00001001)b, (00001011)b, (00001000)b (00001101)b, (00001111)b, (00001100)b
(01100110)b	(00000010)b, (00000011)b, (00000000)b (00001010)b, (00001011)b, (00001000)b (00001110)b, (00001111)b, (00001100)b
(01100111)b	(00000001)b, (00000010)b, (00000011)b, (00000000)b (00001001)b, (00001010)b, (00001011)b, (00001000)b (00001101)b, (00001110)b, (00001111)b, (00001100)b
(01110000)b	(00000000)b (00000100)b (00001000)b (00001100)b
(01110001)b	(00000001)b, (00000000)b (00000101)b, (00000100)b (00001001)b, (00001000)b (00001101)b, (00001100)b

TA(1)	Valid parameter setting for PPS1
(01110010)b	(00000010)b, (00000000)b (00000110)b, (00000100)b (00001010)b, (00001000)b (00001110)b, (00001100)b
(01110011)b	(00000001)b, (00000010)b, (00000000)b (00000101)b, (00000110)b, (00000100)b (00001001)b, (00001010)b, (00001000)b (00001101)b, (00001110)b, (00001100)b
(01110100)b	(00000011)b, (00000000)b (00000111)b, (00000100)b (00001011)b, (00001000)b (00001111)b, (00001100)b
(01110101)b	(00000001)b, (00000011)b, (00000000)b (00000101)b, (00000111)b, (00000100)b (00001001)b, (00001011)b, (00001000)b (00001101)b, (00001111)b, (00001100)b
(01110110)b	(00000010)b, (00000011)b, (00000000)b (00000110)b, (00000111)b, (00000100)b (00001010)b, (00001011)b, (00001000)b (00001110)b, (00001111)b, (00001100)b
(01110111)b	(00000001)b, (00000010)b, (00000011)b, (00000000)b (00000101)b, (00000110)b, (00000111)b, (00000100)b (00001001)b, (00001010)b, (00001011)b, (00001000)b (00001101)b, (00001110)b, (00001111)b, (00001100)b
[a] PPS command is useless in this case and may not be supported by the PICC.	

Scenario J.1 —High bit rate selection, Type A, Procedure 1

PCD		PCD-test-apparatus
RATS command frame ('E0 01' CRC_A)	→	
	←	ATS, TA(1) according to Table J.1 — Correct behaviour of PCD after ATS with TA(1)
Optional PPS request according to Table J.1 — Correct behaviour of PCD after ATS with TA(1)	→	
	←	PPS response (using bit rate fc/128)
$I(0)_0$ (using selected bit rate)	→	
	←	$I(0)_0$ **(using selected bit rate)**
S(DESELECT) request	→	
	←	S(DESELECT) **response** (using selected bit rate)
WUPA (using bit rate fc/128)	→	
	←	ATQA (using bit rate fc/128)

J.2.1.1 Expected result

The PCD shall behave as described in Scenario J.1 in each of the 72 test cases.

J.2.1.2 Test report

If the PCD behaves valid according to Scenario J.1 in each of the 72 test cases, then this test passed. The test report should document the bit rates chosen by the PCD in each of the 72 test cases.

J.2.2 Procedure for Type B

The following procedure shall be repeated for all values of the protocol info byte Bit_Rate_capability defined in Table J.2 — Correct behaviour of PCD after ATQB:

a) The PCD shall send a valid REQB Command frame.

b) The PCD-test-apparatus answers with a valid ATQB including Bit_Rate_capability byte according to Table J.2 — Correct behaviour of PCD after ATQB.

c) The PCD shall send an ATTRIB command with a valid parameter setting for Param2 byte according to Table J.2 — Correct behaviour of PCD after ATQB.

d) The PCD-test-apparatus acknowledges the received ATTRIB with a valid Answer to ATTRIB Command.

e) PCD shall send $I(0)_0$ block using the bit rate selected with Param2.

NOTE This block may also be $I(1)_0$, or R(NAK) in case of PICC presence check method 2a.

f) The PCD-test-apparatus sends a valid response using the bit rate selected with Param2. Check, if the answer from the PCD-test apparatus is accepted by the PCD.

NOTE The following steps may not be applicable when a PCD is embedded in a product:

g) The PCD shall send an S(DESELECT) request using the bit rate selected.

h) The PCD-test-apparatus sends a valid S(DESELECT) response using the bit rate selected. Check, if the answer from the PCD-test apparatus is accepted by the PCD.

i) The PCD shall send a valid REQB Command frame using the bit rate fc/128.

j) PCD-test-apparatus answers with a valid ATQB including Bit_Rate_capability byte according to Table J.2 — Correct behaviour of PCD after ATQB.

Table J.2 — Correct behaviour of PCD after ATQB

Bit_Rate_capability	Valid parameter setting for Param2 [a]
(10000000)b	(0000xxxx)b
(10010001)b	(0101xxxx)b, (0000xxxx)b
(10100010)b	(1010xxxx)b, (0000xxxx)b
(10110011)b	(0101xxxx)b, (1010xxxx)b, (0000xxxx)b
(11000100)b	(1111xxxx)b, (0000xxxx)b
(11010101)b	(0101xxxx)b, (1111xxxx)b, (0000xxxx)b
(11100110)b	(1010xxxx)b, (1111xxxx)b, (0000xxxx)b
(11110111)b	(0101xxxx)b, (1010xxxx)b, (1111xxxx)b, (0000xxxx)b
(00000000)b	(0000xxxx)b
(00000001)b	(0001xxxx)b, (0000xxxx)b
(00000010)b	(0010xxxx)b, (0000xxxx)b
(00000011)b	(0001xxxx)b, (0010xxxx)b, (0000xxxx)b
(00000100)b	(0011xxxx)b, (0000xxxx)b
(00000101)b	(0001xxxx)b, (0011xxxx)b, (0000xxxx)b
(00000110)b	(0010xxxx)b, (0011xxxx)b, (0000xxxx)b
(00000111)b	(0001xxxx)b, (0010xxxx)b, (0011xxxx)b, (0000xxxx)b
(00010000)b	(0000xxxx)b (0100xxxx)b
(00010001)b	(0001xxxx)b, (0000xxxx)b (0101xxxx)b, (0100xxxx)b
(00010010)b	(0010xxxx)b, (0000xxxx)b (0110xxxx)b, (0100xxxx)b

Bit_Rate_capability	Valid parameter setting for Param2 [a]
(00010011)b	(0001xxxx)b, (0010xxxx)b, (0000xxxx)b (0101xxxx)b, (0110xxxx)b, (0100xxxx)b
(00010100)b	(0011xxxx)b, (0000xxxx)b (0111xxxx)b, (0100xxxx)b
(00010101)b	(0001xxxx)b, (0011xxxx)b, (0000xxxx)b (0101xxxx)b, (0111xxxx)b, (0100xxxx)b
(00010110)b	(0010xxxx)b, (0011xxxx)b, (0000xxxx)b (0110xxxx)b, (0111xxxx)b, (0100xxxx)b
(00010111)b	(0001xxxx)b, (0010xxxx)b, (0011xxxx)b, (0000xxxx)b (0101xxxx)b, (0110xxxx)b, (0111xxxx)b, (0100xxxx)b
(00100000)b	(0000xxxx)b (1000xxxx)b
(00100001)b	(0001xxxx)b, (0000xxxx)b (1001xxxx)b, (1000xxxx)b
(00100010)b	(0010xxxx)b, (0000xxxx)b (1010xxxx)b, (1000xxxx)b
(00100011)b	(0001xxxx)b, (0010xxxx)b, (0000xxxx)b (1001xxxx)b, (1010xxxx)b, (1000xxxx)b
(00100100)b	(0011xxxx)b, (0000xxxx)b (1011xxxx)b, (1000xxxx)b
(00100101)b	(0001xxxx)b, (0011xxxx)b, (0000xxxx)b (1001xxxx)b, (1011xxxx)b, (1000xxxx)b
(00100110)b	(0010xxxx)b, (0011xxxx)b, (0000xxxx)b (1010xxxx)b, (1011xxxx)b, (1000xxxx)b
(00100111)b	(0001xxxx)b, (0010xxxx)b, (0011xxxx)b, (0000xxxx)b (1001xxxx)b, (1010xxxx)b, (1011xxxx)b, (1000xxxx)b
(00110000)b	(0000xxxx)b (0100xxxx)b (1000xxxx)b
(00110001)b	(0001xxxx)b, (0000xxxx)b (0101xxxx)b, (0100xxxx)b (1001xxxx)b, (1000xxxx)b
(00110010)b	(0010xxxx)b, (0000xxxx)b (0110xxxx)b, (0100xxxx)b (1010xxxx)b, (1000xxxx)b
(00110011)b	(0001xxxx)b, (0010xxxx)b, (0000xxxx)b (0101xxxx)b, (0110xxxx)b, (0100xxxx)b (1001xxxx)b, (1010xxxx)b, (1000xxxx)b
(00110100)b	(0011xxxx)b, (0000xxxx)b (0111xxxx)b, (0100xxxx)b (1011xxxx)b, (1000xxxx)b
(00110101)b	(0001xxxx)b, (0011xxxx)b, (0000xxxx)b (0101xxxx)b, (0111xxxx)b, (0100xxxx)b (1001xxxx)b, (1011xxxx)b, (1000xxxx)b
(00110110)b	(0010xxxx)b, (0011xxxx)b, (0000xxxx)b (0110xxxx)b, (0111xxxx)b, (0100xxxx)b (1010xxxx)b, (1011xxxx)b, (1000xxxx)b
(00110111)b	(0001xxxx)b, (0010xxxx)b, (0011xxxx)b, (0000xxxx)b (0101xxxx)b, (0110xxxx)b, (0111xxxx)b, (0100xxxx)b (1001xxxx)b, (1010xxxx)b, (1011xxxx)b, (1000xxxx)b

Bit_Rate_capability	Valid parameter setting for Param2 [a]
(01000000)b	(0000xxxx)b (1100xxxx)b
(01000001)b	(0001xxxx)b, (0000xxxx)b (1101xxxx)b, (1100xxxx)b
(01000010)b	(0010xxxx)b, (0000xxxx)b (1110xxxx)b, (1100xxxx)b
(01000011)b	(0001xxxx)b, (0010xxxx)b, (0000xxxx)b (1101xxxx)b, (1110xxxx)b, (1100xxxx)b
(01000100)b	(0011xxxx)b, (0000xxxx)b (1111xxxx)b, (1100xxxx)b
(01000101)b	(0001xxxx)b, (0011xxxx)b, (0000xxxx)b (1101xxxx)b, (1111xxxx)b, (1100xxxx)b
(01000110)b	(0010xxxx)b, (0011xxxx)b, (0000xxxx)b (1110xxxx)b, (1111xxxx)b, (1100xxxx)b
(01000111)b	(0001xxxx)b, (0010xxxx)b, (0011xxxx)b, (0000xxxx)b (1101xxxx)b, (1110xxxx)b, (1111xxxx)b, (1100xxxx)b
(01010000)b	(0000xxxx)b (0100xxxx)b (1100xxxx)b
(01010001)b	(0001xxxx)b, (0000xxxx)b (0101xxxx)b, (0100xxxx)b (1101xxxx)b, (1100xxxx)b
(01010010)b	(0010xxxx)b, (0000xxxx)b (0110xxxx)b, (0100xxxx)b (1110xxxx)b, (1100xxxx)b
(01010011)b	(0001xxxx)b, (0010xxxx)b, (0000xxxx)b (0101xxxx)b, (0110xxxx)b, (0100xxxx)b (1101xxxx)b, (1110xxxx)b, (1100xxxx)b
(01010100)b	(0011xxxx)b, (0000xxxx)b (0111xxxx)b, (0100xxxx)b (1111xxxx)b, (1100xxxx)b
(01010101)b	(0001xxxx)b, (0011xxxx)b, (0000xxxx)b (0101xxxx)b, (0111xxxx)b, (0100xxxx)b (1101xxxx)b, (1111xxxx)b, (1100xxxx)b
(01010110)b	(0010xxxx)b, (0011xxxx)b, (0000xxxx)b (0110xxxx)b, (0111xxxx)b, (0100xxxx)b (1110xxxx)b, (1111xxxx)b, (1100xxxx)b
(01010111)b	(0001xxxx)b, (0010xxxx)b, (0011xxxx)b, (0000xxxx)b (0101xxxx)b, (0110xxxx)b, (0111xxxx)b, (0100xxxx)b (1101xxxx)b, (1110xxxx)b, (1111xxxx)b, (1100xxxx)b
(01100000)b	(0000xxxx)b (1000xxxx)b (1100xxxx)b
(01100001)b	(0001xxxx)b, (0000xxxx)b (1001xxxx)b, (1000xxxx)b (1101xxxx)b, (1100xxxx)b
(01100010)b	(0010xxxx)b, (0000xxxx)b (1010xxxx)b, (1000xxxx)b (1110xxxx)b, (1100xxxx)b

Bit_Rate_capability	Valid parameter setting for Param2 [a]
(01100011)b	(0001xxxx)b, (0010xxxx)b, (0000xxxx)b (1001xxxx)b, (1010xxxx)b, (1000xxxx)b (1101xxxx)b, (1110xxxx)b, (1100xxxx)b
(01100100)b	(0011xxxx)b, (0000xxxx)b (1011xxxx)b, (1000xxxx)b (1111xxxx)b, (1100xxxx)b
(01100101)b	(0001xxxx)b, (0011xxxx)b, (0000xxxx)b (1001xxxx)b, (1011xxxx)b, (1000xxxx)b (1101xxxx)b, (1111xxxx)b, (1100xxxx)b
(01100110)b	(0010xxxx)b, (0011xxxx)b, (0000xxxx)b (1010xxxx)b, (1011xxxx)b, (1000xxxx)b (1110xxxx)b, (1111xxxx)b, (1100xxxx)b
(01100111)b	(0001xxxx)b, (0010xxxx)b, (0011xxxx)b, (0000xxxx)b (1001xxxx)b, (1010xxxx)b, (1011xxxx)b, (1000xxxx)b (1101xxxx)b, (1110xxxx)b, (1111xxxx)b, (1100xxxx)b
(01110000)b	(0000xxxx)b (0100xxxx)b (1000xxxx)b (1100xxxx)b
(01110001)b	(0001xxxx)b, (0000xxxx)b (0101xxxx)b, (0100xxxx)b (1001xxxx)b, (1000xxxx)b (1101xxxx)b, (1100xxxx)b
(01110010)b	(0010xxxx)b, (0000xxxx)b (0110xxxx)b, (0100xxxx)b (1010xxxx)b, (1000xxxx)b (1110xxxx)b, (1100xxxx)b
(01110011)b	(0001xxxx)b, (0010xxxx)b, (0000xxxx)b (0101xxxx)b, (0110xxxx)b, (0100xxxx)b (1001xxxx)b, (1010xxxx)b, (1000xxxx)b (1101xxxx)b, (1110xxxx)b, (1100xxxx)b
(01110100)b	(0011xxxx)b, (0000xxxx)b (0111xxxx)b, (0100xxxx)b (1011xxxx)b, (1000xxxx)b (1111xxxx)b, (1100xxxx)b
(01110101)b	(0001xxxx)b, (0011xxxx)b, (0000xxxx)b (0101xxxx)b, (0111xxxx)b, (0100xxxx)b (1001xxxx)b, (1011xxxx)b, (1000xxxx)b (1101xxxx)b, (1111xxxx)b, (1100xxxx)b
(01110110)b	(0010xxxx)b, (0011xxxx)b, (0000xxxx)b (0110xxxx)b, (0111xxxx)b, (0100xxxx)b (1010xxxx)b, (1011xxxx)b, (1000xxxx)b (1110xxxx)b, (1111xxxx)b, (1100xxxx)b
(01110111)b	(0001xxxx)b, (0010xxxx)b, (0011xxxx)b, (0000xxxx)b (0101xxxx)b, (0110xxxx)b, (0111xxxx)b, (0100xxxx)b (1001xxxx)b, (1010xxxx)b, (1011xxxx)b, (1000xxxx)b (1101xxxx)b, (1110xxxx)b, (1111xxxx)b, (1100xxxx)b

[a] The least significant half byte of Param2 is used to code the maximum frame size that can be received by the PCD.

Scenario J.2 —High bit rate selection, Type B, Procedure 2

PCD		PCD-test-apparatus
REQB ('05 00 00' CRC_B)	→	
	←	ATQB, Bit_Rate_capability according to Table J.2 — Correct behaviour of PCD after ATQB
ATTRIB command, Param2 according to Table J.2 — Correct behaviour of PCD after ATQB	→	
	←	Answer to ATTRIB command (using bit rate fc/128)
$I(0)_0$ (using selected bit rate)	→	
	←	$I(0)_0$ (using selected bit rate)
S(DESELECT) request	→	
	←	S(DESELECT) response (using selected bit rate)
WUPB (using bit rate fc/128)	→	
	←	ATQB (using bit rate fc/128)

J.2.2.1 Expected result

The PCD shall behave as described in Scenario J.2 in each of the 72 test cases.

J.2.2.2 Test report

If the PCD behaves valid according to Scenario J.2 in each of the 72 test cases, then this test passed. The test report should document the bit rates chosen by the PCD in each of the 72 test cases.

Bibliography

[1] ISO/IEC 9646-1:1994, *Information technology — Open Systems Interconnection — Conformance testing methodology and framework — Part 1: General concepts*

[2] ISO/IEC 9646-2:1994, *Information technology — Open Systems Interconnection — Conformance testing methodology and framework — Part 2: Abstract Test Suite specification*

[3] ISO/IEC 9646-3:1998, *Information technology — Open Systems Interconnection — Conformance testing methodology and framework — Part 3: The Tree and Tabular Combined Notation (TTCN)*

[4] ISO/IEC 9646-4:1994, *Information technology — Open Systems Interconnection — Conformance testing methodology and framework — Part 4: Test realization*

[5] ISO/IEC 9646-5:1994, *Information technology — Open Systems Interconnection — Conformance testing methodology and framework — Part 5: Requirements on test laboratories and clients for the conformance assessment process*

[6] ISO/IEC 9646-6:1994, *Information technology — Open Systems Interconnection — Conformance testing methodology and framework — Part 6: Protocol profile test specification*

[7] ISO/IEC 9646-7:1995, *Information technology — Open Systems Interconnection — Conformance testing methodology and framework — Part 7: Implementation Conformance Statements*